Plasma etch fabrication of 60:1 aspect ratio silicon nanogratings with 200 nm pitch

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The authors present a breakthrough multistage dry-etch process to create 100 nm half-pitch gratings in silicon with depths up to 6 μm. Interference lithography was used to pattern gratings in an optically matched stack of materials to form a 400-nm-thick silicon oxide hard-mask. The oxide was then used to mask the subsequent deep reactive-ion etching of silicon. In this article, the authors describe their grating patterning, pattern transfer, and deep etch processes, and present progress toward combining this technique with coarser scale lithography steps designed to form an integrated mechanical support structure to produce freestanding x-ray diffraction gratings. © *2010 American Vacuum Society.* [DOI: 10.1116/1.3507427]

I. INTRODUCTION

Nanoscale silicon gratings have a variety of applications to both ground- and space-based sensors. Ultraviolet filtration on the medium energy neutral atom instrument for the IMAGE satellite was accomplished by gold gratings with 40 nm slits and 510 nm thickness.[1–3] Similar gratings were used in experiments with extreme ultraviolet (EUV) diffraction[4] and 0.5 keV electron diffraction.[5,6] High resolution x-ray spectroscopy on NASA's Chandra Space Telescope was enabled by 200 and 400 nm period gratings suspended on submicrometer thickness polyimide membranes.[7]

The next step in space-based x-ray telescopes will be taken by Chandra's successor, the International X-ray Observatory (IXO). The science requirements for IXO demand diffraction gratings with specifications and tolerances not easily achieved by traditional transmission or reflection gratings. We have developed a new kind of diffraction grating that has the advantages of both transmission and reflection gratings while avoiding their disadvantages. Called critical-angle transmission (CAT) gratings, they require freestanding, extremely high aspect ratio (>100) silicon grating bars with very smooth sidewalls and a feature pitch on the order of a few hundred nanometers.[8–10] The fabrication work in this article was performed with CAT grating fabrication in mind, but the etch techniques are general enough to be used for other applications.

In CAT gratings, x-rays are transmitted through vacuum and the path length differences that lead to diffraction are generated via grazing-incidence reflection off the ultrasmooth sidewalls of high aspect ratio grating bars. The x-ray incidence angle must be below the critical angle of total external reflection in order to achieve high diffraction efficiency. This is accomplished by tilting the grating normal by a small angle relative to the incident photons. CAT gratings can therefore achieve diffraction efficiencies on the order of 50% over a broad band that rival those of grazing-incidence reflection gratings while still maintaining the low mass and relaxed alignment tolerances of traditional transmission gratings.

In the past, two techniques have been used to create extreme-aspect-ratio silicon gratings with the requisite feature pitch: an oxygen-rich Bosch plasma process[11–13] and an anisotropic wet etch using (110) wafers.[8,14] The former technique was limited to aspect ratios of 15–20 and had problems with micromasking due to sputtering and redeposition of the metal mask, while the latter resulted in aspect ratios up to 150, but with relatively low open area due to buried {111} planes at cross angles to the grating sidewalls.

Our new process solves many of the problems of both prior approaches by combining them. We insert a plasma deep-reactive ion etch (DRIE) step into the wet process, which removes the problem of the buried {111} planes choking off the open grating area. This enables the creation of highly efficient x-ray diffraction gratings and ultraviolet filters. Since the new process uses silicon oxide as a mask for the DRIE step, the micromasking caused by the use of metal masks in the Bosch-only process is also removed.

Careful balancing of etch parameters on a variety of tools allows us to control the duty cycle and aspect ratio of the gratings, etch speed and selectivity, and the profile of grating bars. We have achieved, as a step toward the ideal freestanding gratings, a 200-nm-pitch grating with 50% duty cycle and 6 μm etch depth over a surface greater than 2 cm^2. There was no noticeable scalloping or undercut of the silicon oxide mask. The uniformity of interference lithography and the control allowed by advanced dry-etch tools result in a very repeatable process that creates templates that can be further tailored for a variety of applications. For the CAT gratings, further grating bar smoothing, duty cycle reduction, and aspect ratio tailoring will be accomplished by a subsequent wet polish similar to that used by Ahn *et al.*[8]

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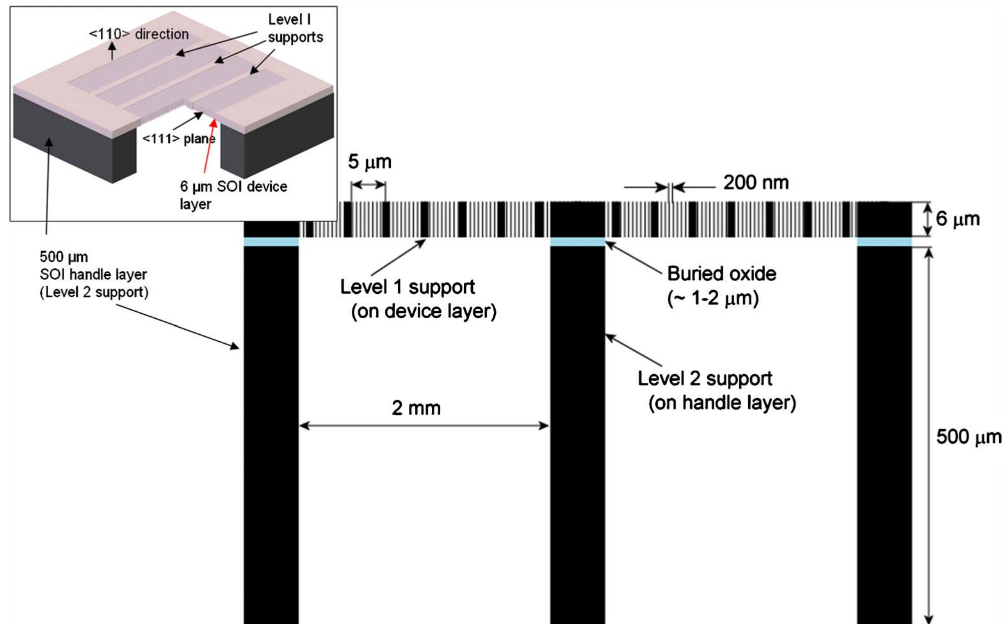

FIG. 1. (Color online) Device schematic. The 40–50 nm wide, 6 μm deep grating bars are defined by the vertical {111} planes in (110) silicon. The 300–500 nm wide Level 1 support bars in the device layer lie across the grating bars for stiffness and location fidelity. The 50–100 μm wide Level 2 supports are the full thickness of the handle layer and follow a honeycomb pattern for maximum structural rigidity.

II. FABRICATION SUMMARY

Freestanding gratings require the use of silicon-on-insulator (SOI) wafers. Each wafer has a 6.25 μm top silicon device layer, a 2 μm buried insulator layer for etch stopping, and a 500–550 μm silicon handle substrate. Figure 1 shows a schematic of the CAT grating device, including both the device layer (Level 1) supports that keep the grating bars straight and parallel, and the handle layer (Level 2) supports used for additional large-scale structural stability. Our fabrication is now in transition from a wet chemical process to a combined wet and dry process, and as such, certain elements are further along the development cycle than others. We are testing front and back etching separately at the moment, but we have a path laid out for full integration. The complete process flow is shown in Fig. 2 and is described below, but the primary focus of this article con-

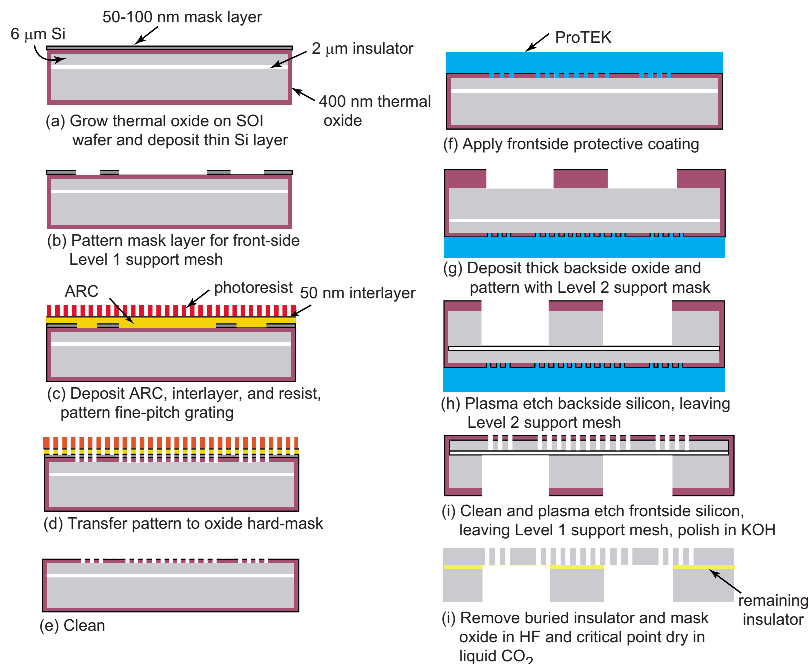

FIG. 2. (Color online) Fabrication process flow.

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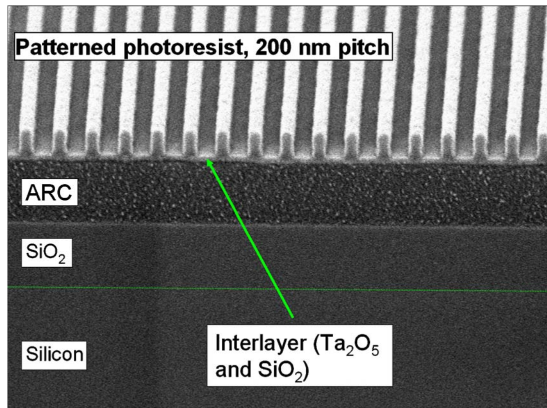

FIG. 3. (Color online) Electron micrograph of trilayer lithography stack. The photoresist is exposed to interference lithography from a 351 nm laser, and the interlayer and ARC are used to transfer the pattern to the SiO_2 hard-mask shown in Fig. 4.

TABLE I. Etch parameters for pattern transfer from photoresist to oxide hard-mask.

Etch parameter	Interlayer etch	ARC etch	SiO_2 etch
H_2 Flow rate (SCCM[a])	25	0	15
CF_4 Flow rate (SCCM)	25	0	25
O_2 Flow rate (SCCM)	0	50	0
ECR power (W)	96	45	96
Bias (V)	612	480	420
Pressure (mTorr)	10	7	10
Chuck temperature (°C)	30	30	30
Time (s)	105	165	1100

[a]"SCCM" is measure of gas flow that stands for standard cubic centimeters per minute.

cerns steps (c)–(e) and the first part of (i), the masking and dry etching of high aspect ratio silicon gratings.

After initial cleaning, 400 nm of thermal oxide is grown on the wafer to serve as a mask for the grating. On the device side, a layer of material is deposited and patterned with the Level 1 support mask that lies across the direction of the primary grating. In our prior wet process, we used chromium for this mask material. We are currently exploring options for this layer such as polysilicon, silicon nitride, or titanium or a similar metal with low sputtering yield. The primary criteria are ease of patterning and low sputtering yield in the energetic oxide etch. We used a 1 μm layer of PFI-88a2 photoresist (Sumitomo Corporation) for our initial tests, but this was deposited and patterned after the grating mask rather than before, and the resist receded during the deep silicon etch, resulting in a tapered profile for the support bars.

To transfer the primary grating pattern to the SiO_2 hard-mask, a three layer stack of materials is used in a process very similar to that first demonstrated by Schattenburg *et al.*[15] First, a 400 nm layer of anti-reflective coating (ARC) (BARLi, AZ Electronics Materials) is spin-coated atop the Level 1 support mask. Then an interlayer composed of 15 nm of SiO_2 and 15 nm of Ta_2O_5 is evaporated onto the surface by a Temescal VES-2550 evaporator, and finally, 200 nm of PFI-88a2 photoresist is applied by spin-coating.

The photoresist is patterned with interference lithography using a 351 nm argon ion laser at a 200 nm pitch with approximately 45% duty cycle, as shown in Fig. 3. The CAT grating and Level 1 support grating patterns are transferred to the thermal SiO_2 layer by a Plasmaquest Series II Reactor model 145, an electron cyclotron resonance (ECR) reactive ion etcher, using the etch parameters shown in Table I. The resultant hard-mask is shown in Fig. 4. Then, the wafer is cleaned in a piranha solution (equal mixture of H_2SO_4 and H_2O_2) to remove any remaining ARC, and a thick layer of ProTEK™ protective coating (Brewer Science, Inc.) is spin-coated on for surface protection.

The back-side handle layer pattern is the Level 2 support structure, a 1–2 mm period honeycomb with 5% duty cycle. We are currently performing tests to determine the optimal period and etch parameters. The patterning process for this will be by standard photolithography (Karl Suss Model MA-6 mask aligner) and dry etch.

Full device integration will require the etching of both sides of the SOI wafer. First, the handle layer will be etched by an inductively coupled plasma tool running a standard SF_6/C_4F_8 Bosch DRIE process. In the process used by Mukherjee *et al.*,[13] the through-wafer etch stops on the buried insulator layer after approximately 3 h, but newer tools will be approximately six times faster. After the back etch is complete, the ProTEK™ layer will be removed with a solvent soak and a short oxygen plasma etch, and then the high aspect ratio grating etch will be performed in a STS Pegasus DRIE tool using the parameters shown in Table II.

Since the dry etch alone does not result in grating bars smooth enough to enable the necessary specular x-ray reflection, it must still be followed by a short wet etch similar to that used by Ahn *et al.*[8] This means that the grating bars still need to be perfectly aligned with the vertical {111} planes of (110) silicon wafers. It also means that the residue from the DRIE step needs to be removed in order to expose the silicon

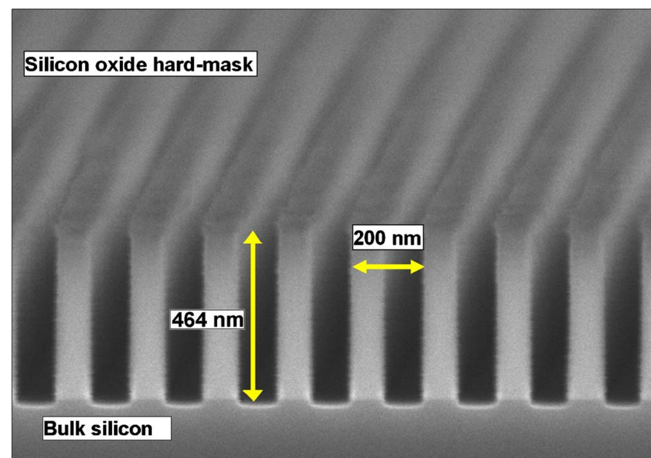

FIG. 4. (Color online) Electron micrograph of oxide mask after step (e) in Fig. 2. The duty cycle of the mask is 50% and the aspect ratio of the bars is close to 5:1. The oxide masks the grating DRIE to result in the silicon gratings shown in Figs. 7 and 8.

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TABLE II. Grating DRIE parameters.

Device parameter	Deposition cycle	Etch cycle
SF_6 Flow rate (SCCM)	0	200
C_4F_8 Flow rate (SCCM)	150	80
Coil power (W)	2000	1100
Platen power (W)	0	30–60[a]
Cycle time (s)	1	1.5
Base pressure (mTorr)	7.5	
Chuck temperature (°C)	−15	

[a]Linear ramp over 12 min.

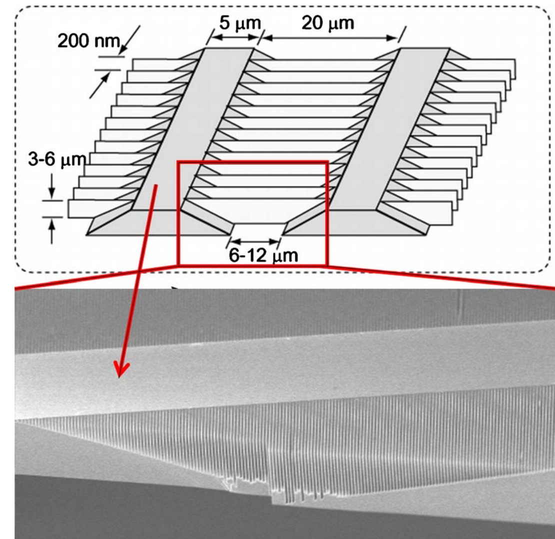

FIG. 5. (Color online) Schematic and electron micrograph of grating geometry using KOH wet etching process. Top: schematic of CAT gratings (white) and Level 1 supports (gray). X rays are incident from the top. Bottom: electron micrograph of cleaved section demonstrating the inward slope of the buried {111} planes.

to the chemical etch. The latter can be accomplished through either plasma or wet chemical processing, and both methods are under investigation.

It is very important that neither DRIE step penetrate through the buried layer because the subsequent wet processing requires a contiguous dielectric etch stop. The wet polish step is in room temperature potassium hydroxide (KOH) and should take only a few minutes rather than the hours required by the process of Ahn *et al.* Then, the wafer will be transfered to a hydrofluoric acid (HF) solution to remove the buried layer and masks, and from there, it will go to the critical-point dryer. At no point during these wet etch steps or the water rinses in between will the gratings ever be exposed to air due to stiction concerns. Again, we have not completed this full process integration, but each step has been performed in prior iterations of the process.

For applications other than CAT gratings, the buried oxide layer is removed after the back-side DRIE using a short fluorocarbon plasma etch with high selectivity to silicon. This allows the relaxation of any buckling caused by the buried oxide's compressive stress. The grating DRIE step then results in freestanding gratings with no need for wet processing.

III. PROCESS DISCUSSION AND RESULTS

CAT gratings require very tall, thin, nanometer-smooth grating bars and a large geometric area unobstructed by supports. The former requirement has been met in the past through the use of (110) silicon SOI wafers. The 200 nm grating pattern was carefully aligned to the vertical {111} planes of the device layer surface using the fan-pattern process demonstrated by Ahn *et al.*,[8] and a KOH wet etch transferred the pattern, providing almost atomically flat grating bars. However, as Fig. 5 demonstrates, the grating support bars widened along the buried {111} planes, closing off the bottom surface and resulting in very low usable CAT grating area. In order to resolve this problem, we have changed the fabrication flow to use plasma processing for both the front- and back-side etches followed by a short KOH etch to narrow and polish the grating bars.

Unfortunately, the selectivity of DRIE tools does not match that of a chemical etch. The prior wet process used a very thin silicon nitride masking layer for the full grating etch, but the dry process requires a fairly thick, high aspect ratio silicon oxide mask.

A great deal of development went into the lithography and etching of the oxide hard-mask, both in terms of optical matching of the material stack and determination of the optimal etch parameters as detailed in Table I. The thick ARC was critical to this process since it both prevents optical waves from reflecting back into the photoresist during interference lithography and acts as an etch mask for the underlying SiO_2. The interlayer, consisting of both SiO_2 and Ta_2O_5, also serves two purposes: it approximately matches the index of refraction for the resist and ARC, which reduces reflected waves, and it provides an etch mask for the ARC that is highly selective in an oxygen plasma.

The oxides of both the interlayer and the hard-mask are etched with a mixture of H_2 and CF_4. The H_2 passivates the etch and increases the selectivity to oxide when using a polymer mask. This passivation increases the duty cycle of the mask by a few percent, but there is a risk of the polymer mask becoming misshapen and/or collapsing. The cause of this is uncertain, but we hypothesize that it was due to overheating. Since the photoresist masking the interlayer has an aspect ratio of approximately 2:1, it is a stable structure that is resistant to deformation and thus a high H_2 flow was used during the interlayer etch for maximum passivation. This increased the duty cycle of the interlayer slightly, allowing for some margin of undercutting during the subsequent ARC etch. The ARC is etched at the lowest possible pressure to maximize the sidewall straightness since an aspect ratio of 4:1 is required. During the hard-mask etch, both the H_2 flow and the bias voltage are reduced to prevent mask damage during the etch. The selectivity of the oxide etch was close to

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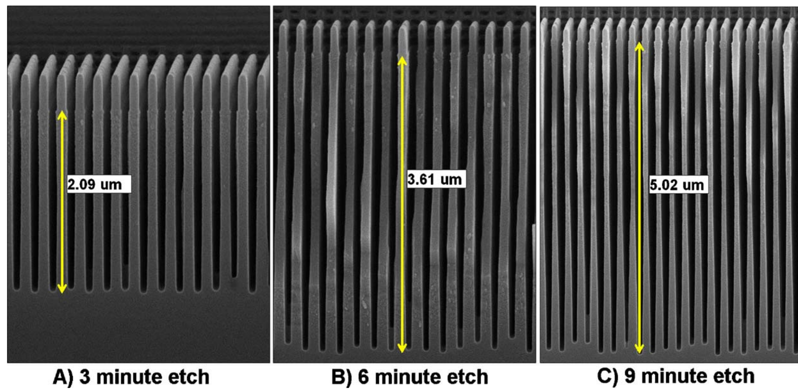

FIG. 6. (Color online) Electron micrographs of the silicon grating after (a) 3, (b) 6, and (c) 9 min of DRIE in a STS Pegasus tool.

unity, since little mask remained after the etch, but it provided a mask with a 50% duty cycle as seen in Fig. 4.

We began DRIE process development on the STS Pegasus tool by setting the shortest possible etch and deposition cycle times. This is a critical factor in minimizing the sidewall scalloping. In addition, we reduced the platen temperature to −15 °C to further reduce sidewall etching. While a cryogenic, nonpassivated etch is generally performed at −120 °C, the Pegasus was not capable of such temperatures, but the cooling we did bring to bear showed definite signs of profile improvement.

We had a few false starts due to unexpected effects. For example, if any of the ARC remained atop the SiO_2 mask, each mask bar split into a Y-shape that blocked off the slits and completely changed the etch parameters. Also, once the feature depth passed approximately 4 μm, the compressive stress in the oxide mask was enough to cause the bars to buckle and stick together, resulting in some closed channels and others that were twice as wide as desired. Once these issues were resolved (by piranha clean and using support bars, respectively), the development was primarily an exercise in balancing base pressure and platen power ramping. We first determined the lowest stable base pressure we could maintain with such rapid gas switching, since the base pressure determines the ion mean free path and scattering, which, in turn, strongly affect the vertical profile of the trenches. We then found parameters for the platen power ramp, such that we had no undercut of the top of the features and yet still had adequate throughput to etch the bottom of the trenches.

Figure 6 shows the etch progression from 3 to 9 min and Fig. 7 demonstrates the 60:1 aspect ratio grating geometry we achieved after a full 12 min of etching. The bars are completely straight after 3 min of etching, and mostly so after 6 min. By 9 min, there is some bowing in the silicon bars and a slight irregularity in bar depth. The bowing is slightly more pronounced after 12 min, resulting in bars with a waist that is noticeably thinner than the top and bottom of the bars. It should be mentioned here that we expect that the KOH polish will significantly narrow the grating bars. Any vertical bowing and scalloping of the bars result in local bar thickness minima, and the KOH etch is expected to stop at the {111} planes defined by those minima. The bowed bar-waist demonstrated in Fig. 7 is likely the minimum thickness of each bar, and thus, the likeliest thickness for the postpolished bars. This polish will result in significantly higher aspect ratios for the final gratings, at least 100:1 if the polish stops exactly on the waist of the bars. The irregularity in bar depth will not be present when using SOI wafers, since the oxide serves as a concrete etch-stop and guarantees bars of equal depth.

A detailed view of the remaining oxide hard-mask after 12 min of etching can be seen in Fig. 8. The oxide mask is almost entirely gone, but enough remains such that the sidewalls are still vertical.

Some measured etch parameters are shown in Fig. 9. Of a particular note is the fact that while the silicon etch rate continues dropping throughout the etch (as seen in Figs. 6 and 7), the oxide etch rate rises and eventually peaks. A rise in mask etch rate is understandable, since we continue ramp-

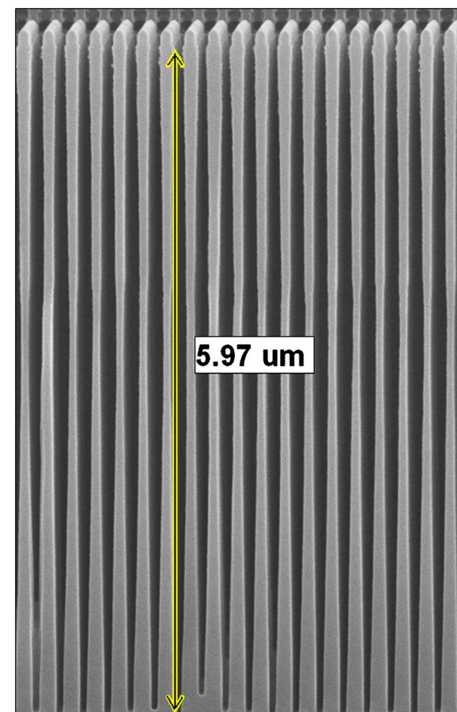

FIG. 7. (Color online) Electron micrograph of silicon grating bars after 12 min of DRIE in a STS Pegasus tool with etch parameters listed in Table II.

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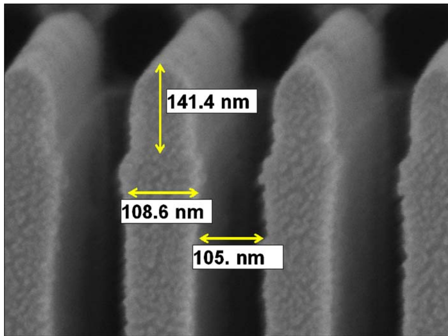

FIG. 8. (Color online) Detail of top of grating bars from Fig. 7. The SiO_2 mask is still vertical and the duty cycle of the grating is 50%.

ing up the platen bias (see Table II), but it is unclear why the etch rate mask would drop toward the end of the etch.

Our integration of grating and bulk-support processes will follow a similar path to the prior development by Mukherjee[11] and will face similar difficulties. In particular, three issues need to be addressed: the vacuum processing of back-etched samples attached to a carrier wafer, heat dissipation during grating DRIE on the suspended structures, and the stress caused by the buried insulation layer.

For CAT gratings, we intend to use (110) silicon with a buried low-stress nitride layer, possibly atop a thicker oxide layer. The advantage of using a nitride layer is that the nitride has a slight tensile stress, resulting in a flat surface after the handle layer etch [step (h) in Fig. 2] instead of the slightly buckled surface that results from having a buried oxide layer. If we use both nitride and oxide, the oxide will provide the stop for the aggressive back-side etch and then be removed prior to the much slower front-side DRIE, leaving the nitride to be etch-stop for both the dry and wet grating etches. For other applications, the standard, and much less expensive, (100) SOI wafers with buried oxide layers can be used, since the buried layer will be removed prior to the primary grating etch.

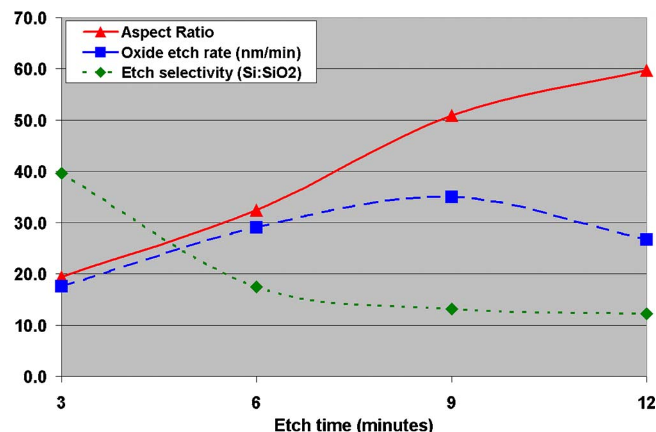

FIG. 9. (Color online) Graph of some measured etch characteristics. The red (triangles) line is the aspect ratio of the silicon trenches, the blue (squares) line is the oxide etch rate in nanometers per minute, and the green (diamonds) line is the etch rate selectivity of silicon vs the oxide mask.

Since DRIE uses relatively dense plasmas, a significant amount of heat is transferred from the plasma to the substrate. In addition, there needs to be a way to vent the atmospheric gas trapped between the carrier wafer and the thin membranes. Both of these issues might be solved by a single innovation: a carrier wafer with slight recesses under each device and through-wafer holes leading to each recess. During vacuum pumpdown, the atmospheric gas filling the honeycomb structure will be removed, and during the DRIE, the cooling helium will fill those chambers and provide a thermal path to cool the surface evenly. This will undergo testing in the near future.

IV. CONCLUSIONS

We have plasma etched nanogratings in bulk silicon with aspect ratios of 60:1, 50% duty cycle, and a pitch of 200 nm. Our future development will result in freestanding gratings with thin fin aspect ratios up to 150 and duty cycles of 10%–15%. These gratings are designed to be used in upcoming space telescopes for x-ray diffraction, but they have an array of other potential uses such as the filtration of UV light, conversion of atomic ions to neutral atoms, birefringent wave plates, particle collimators, polarizers, and trench capacitors.

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