Thermal oxide patterning method for compensating coating stress in silicon X-ray telescope mirrors

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ABSTRACT

Segmented X-ray telescope mirrors fabricated from thin silicon substrates are being developed by a group at the NASA Goddard Space Flight Center for future generation telescopes such as the Lynx mission concept. The Goddard team has demonstrated high precision silicon mirrors with high angular resolution (~1'') manufactured by a simple, low cost process. However, the required high-Z optical coatings on mirror front surfaces are difficult to deposit without significant compressive thin film stress, which threatens to distort mirrors and negate the benefits of the high quality substrates. Coating stress reduction methods have been investigated by several groups, but none to date have reported success on real mirrors to the required tolerances. In this paper, we report a new method for correcting mirrors with stress-induced distortion which utilizes a micro-patterned silicon oxide layer on the mirror's back side. Due to the excellent lithographic precision of the patterning process, we demonstrate stress compensation control to a precision of ~0.3%. The proposed process is simple and inexpensive due to the relatively large pattern features on the photomask. The correction process has been tested on flat silicon wafers with 30 nm-thick chrome coatings under compressive stress and achieved surface slope improvements of a factor of ~80. We have also successfully compensated two iridium-coated silicon mirrors provided by the Goddard group. The RMS slope errors on coated mirrors after compensation were only degraded by ~0.06 arc-seconds RMS axial slope compared to the initial uncoated state.

Keywords: X-ray, silicon mirror, thermal oxide pattern, figure correction, coating stress, stability, low cost

1. INTRODUCTION

The Lynx X-ray telescope mission concept[1] is currently under study for consideration by the 2020 Decadal Review. The mission's ambitious goals include an angular resolution comparable to Chandra (0.5 arc-second) but with some 30X more collecting area and a much wider field of view[2]. A group at the NASA Goddard Space Flight Center has developed a process for producing thin silicon mirrors with high angular resolution (~1'') using a simple, low cost process[3]. These mirrors already come close to meeting requirements for Lynx and rapid progress continues to be made. Unfortunately, preferred mirror reflective coatings, such as iridium, typically exhibit a compressive stress on the order of 1 GPa, which can distort the ~0.5 mm thick mirror's precisely-figured initial shape by many times the tolerance limit[4].

Several groups are working on approaches to mitigate coating-induced mirror distortion, including reducing the coating stress[5,6], coating a stress-balanced layer on the back side[7], patterning electronically adjustable PZT films[8], or implanting ions[9] on the back side to produce a negative shape thus cancelling the distortion. None of these methods to date have reported achieving stable, high precision correction of real telescope mirrors.

We propose a new mitigation technique for compensating mirror coating stress, which calls for first coating the mirror backside with a compensating layer of somewhat higher integrated compressive stress compared to the front side coating[10]. The mirror distortion resulting from stresses in both the front and back side layers is carefully measured, and a finite element model (FEM) is used to calculate the change of a 2D distribution of integrated stress on the back side that would be required to bend the mirror to restore the original figure. Then the back side coating is lithographically patterned and the coating material is partially removed following the prescription of the numerical model, so that the remaining back side stress precisely cancels the front side stress, thus restoring the original mirror figure. For the back side film we chose silicon oxide as discussed below.

Thermal oxidation of silicon wafers is a well-understood process used for electronic chip and MEMS production in the semiconductor industry[11]. Oxide layers are grown on silicon substrates in oxygen with temperatures of ~1000 °C. These films are very uniform and extremely stable with a repeatable ~300 MPa compressive stress due to the volumetric change from Si to SiO_2 and the CTE mismatch between silicon and its oxide. Lithographic processing of SiO_2 is a mature, high precision process, and our implementation is very simple[12]. We chose a pattern based on a tiled array of hexagons with a fixed 500 μm pitch, and a variable duty cycle as a function of position, in order to control the mean local stress. The hexagon duty cycle distribution is determined by FEM using inputs from measured mirror shape errors, mirror size and thickness, and other material and mechanical data[10,13]. The pattern is fabricated by a photo lithographic method followed by etching with HF, which can geometrically be very precise (~1 μm) compared with the hexagon feature sizes (500 μm).

In this paper, we report results of coating stress compensation on 100 mm-diameter, 525 μm-thick flat silicon wafers distorted by 30 nm of chromium[10]. These initial experiments helped to debug the process and elucidate parameters and process steps that need to be controlled for success. In these initial experiments chrome was just a convenient material for study. Once a mature process was developed, we then went on to demonstrate the correction of thin shell (0.7 mm), high fidelity (~1 arc-second) Wolter silicon mirrors produced by the Goddard group which were distorted by 30 nm of iridium coating[14]. The mirrors were successfully restored to their original shapes to within ~0.06 arc-second RMS axial slope.

2. MIRROR CORRECTION PROCESS

The process flow for correcting silicon mirrors is shown in Fig. 1. Starting from high quality silicon mirrors, 200 nm-thick thermal oxide films are grown on both front and back sides in O_2 ambient at 1050 °C (Step 1). This process results in oxide layers with ~300 MPa compressive stress[11], therefore 200 nm thickness will produce ~70 N/m integrated stress, which is just a little larger than the expected integrated stress in the iridium reflective coating applied in Step 3.

After oxidation, the mirror back side is protected by photoresist (Dow SPR-700). The front side oxide is then removed by HF chemical etchant (BOE) and the photoresist is stripped (Step 2). Since the compressive forces on the front side are removed along with the oxide, the substrate is now bowed by the stress in the back side oxide until it reaches mechanical equilibrium. Now the bare front-side silicon surface is sputtered with a 30 nm reflective layer such as iridium (Step 3). An annealing process is followed to reduce and stabilize the coating stress[10] (Step 4). Due to the counter-balancing compressive stress in the oxide coating, the substrate shape is now somewhat recovered, but not quite due to the deliberate overstressing of the back side coating.

During the processes as described above, the relative deformation of flat silicon wafers is monitored by a Shack-Hartmann (S-H) metrology tool in our lab at MIT[15], while that of Wolter silicon mirrors is measured with an interferometer using a cylindrical null by the Goddard group[16]. Based on these measurements, the stress distributions in the back side thermal oxide and in the annealed coating can be precisely determined[10,13,17].

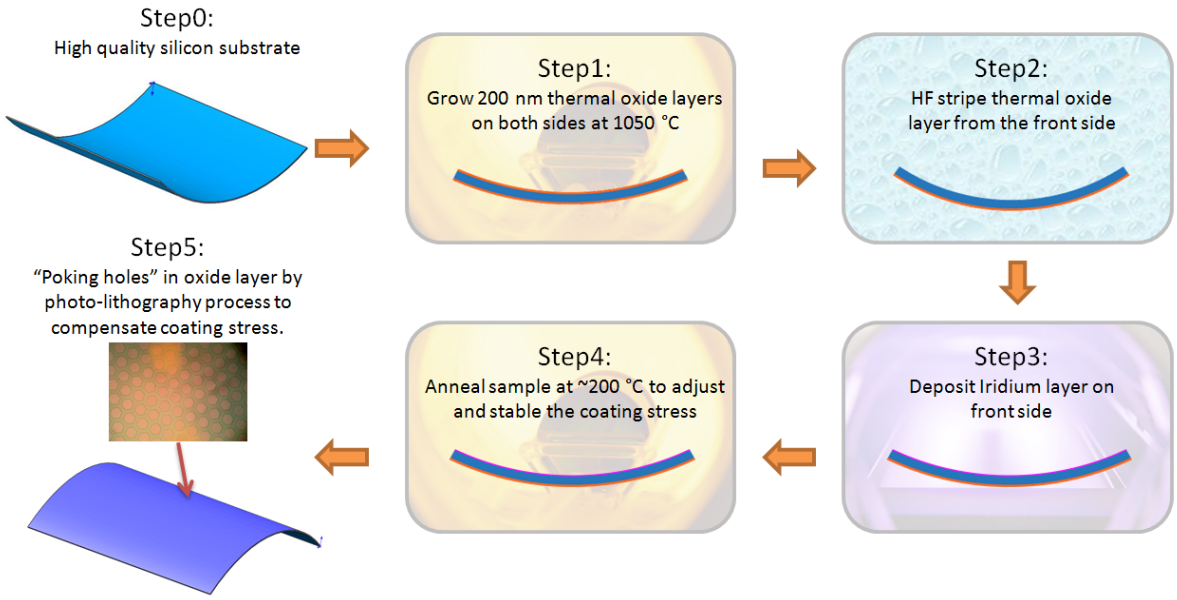

Figure 1. Process flow for thermal oxide patterning stress compensation method

During annealing, as discussed previously, the expected integrated coating stress is adjusted slightly lower than in the oxide. Therefore, the substrate shape will still be slightly distorted due to the integrated stress differential. In order to recover the mirror shape, a photo lithographic process involving BOE etch is applied (Step 5) to create a precise 2D pattern (i.e., poke holes) in the back side oxide film. The pattern is an array of hexagonal holes with 500 μm pitch, where the duty cycle can be individually adjusted within the boundary of each unit cell, as shown in Fig. 2.

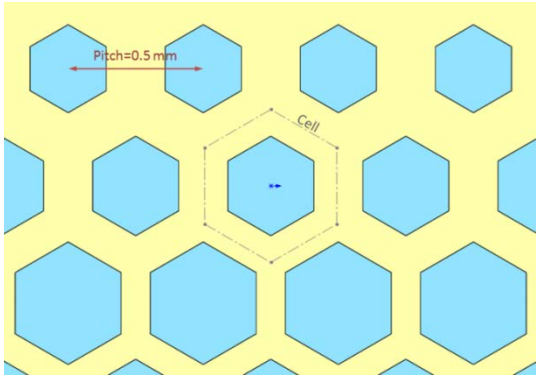

Figure 2.Sketch of hexagon pattern etched into thermal oxide. Blue areas represent bare silicon while gold areas represent oxide.

The hexagon dimensions are chosen to be smaller than the substrate thickness (550 μm for wafers and 700 μm for mirrors), to help suppress local bending moments which could create mid-range figure errors. As a result, the effect of the perforated thermal oxide is equivalent to a thin continuous film of controlled local stress on the back side of the substrate. The equivalent thin film imparts a local integrated stress which is inversely proportional to the areal fraction of oxide that has been removed. The varying area fraction with fixed pitch is similar to a pulse-width modulation (PWM) signal in electronics. The area fraction is defined as a "Duty Cycle" and is calculated by the following equation:

$$Duty\ Cycle\ (X,Y) = \frac{Thermal\ \ Oxide\ \ Stress\ \ (X,Y) - Annealed\ \ \ Coating\ \ Stress\ \ (X,Y)}{Thermal\ \ Oxide\ \ Stress\ \ (X,Y)} \qquad (1)$$

Based on the calculated duty cycle distribution for a specific substrate, such as a silicon wafer or Wolter mirror, a thin-film plastic photomask is produced for subsequent photo lithographic processing.

Figure 3.Photograph of a thin-film plastic photomask designed for 100 mm-diameter silicon wafers. The inset in the upper right corner shows hexagon features as observed under a low-power microscope. The white areas of the mask are UV transparent so that with positive photoresist the exposed areas will be removed.

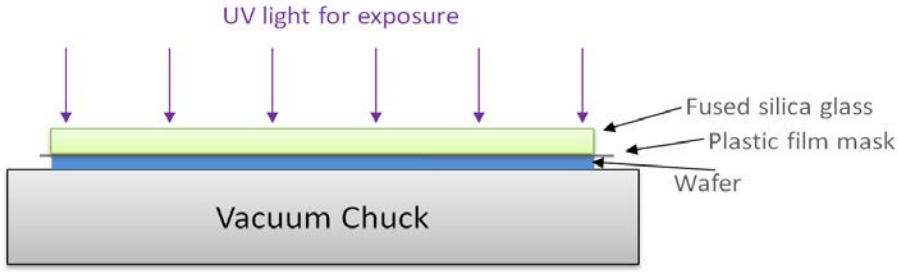

Figure 4. UV light exposure in photo lithography process.

Fig. 3 shows a plastic thin-film mask which is produced by a simple mask writer, which is amenable to low-cost mass production. The upper right corner inset shows hexagon features as observed under a microscope. Fig. 4 represents the exposure step on a flat wafer. The wafer is spin coated by a 1.0 μm-thick layer of Dow SPR-700 photoresist, aligned and then vacuum contacted with the photomask before being exposed with 365 nm UV light. The vacuum ensures intimate contact between photomask and substrate, which is essential for high fidelity pattern transfer. For the curved Wolter mirrors, a custom modified spin coater and alignment tool were developed. The photomask is manually aligned to the substrate, pulled down by a vacuum bag, and then exposed to UV (see Fig. 5).

When the exposure is completed, the sample is dipped into CD-26 developer, rinsed, and the substrate is etched in BOE solution to create the oxide pattern. Since the pattern is calculated by Eq. 1 and produced by the processes above, the local integrated stress on the back side of the substrate will be modulated identically with the duty cycle in the oxide pattern. Subsequently, the distortion induced by the front side coating should be eliminated. Fig. 6 shows a Wolter mirror made by the Goddard group with a thermal oxide hexagon pattern on the back side.

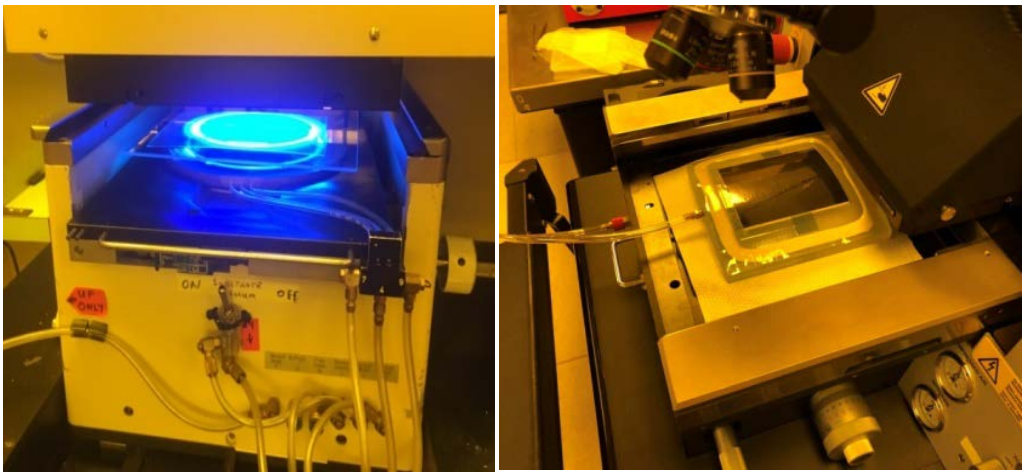

Figure 5. Left: Flat wafer undergoing photomask exposure. Right: Wolter mirror aligned with a mask and pressed by a vacuum bag in the exposure tool.

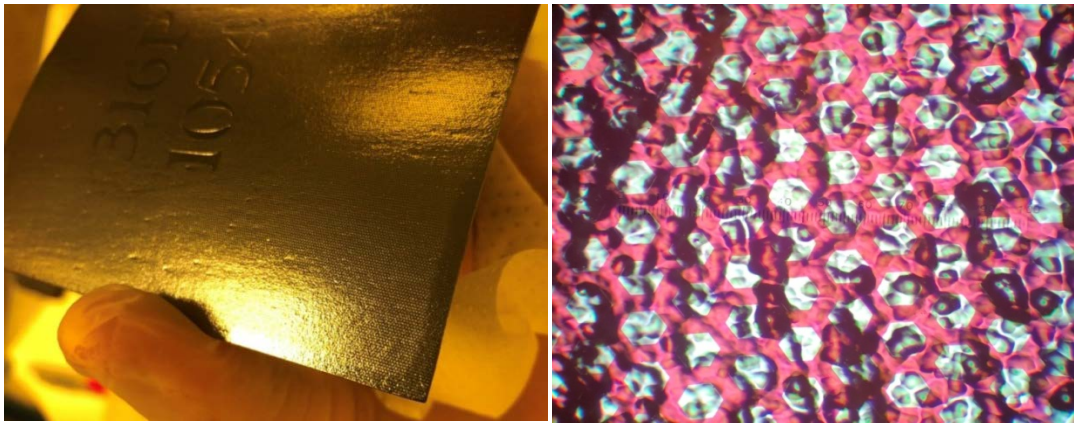

Figure 6. (Left) Thermal oxide hexagon pattern on the back side of a curved Wolter mirror. The hexagonal pattern is most clearly visible in the lower right corner. (Right) Hexagon pattern observed under a low power microscope. Rough marks left over from back side grinding are visible in the image. These do not seem to cause any deleterious effects.

In Fig. 6 (right), the thermal oxide appears to be red, perhaps due to contamination when mirror front side was coated with iridium. Although the back side of the mirror is very rough, the oxide pattern was created successfully.

3. OXIDE STRESS CALIBRATION

A calibration process was performed to understand the precision of stress control that could be achieved using the thermal oxide patterning method. A set of 15 100 mm-diameter silicon wafers with single-side oxide coatings was divided into three groups and the oxide uniformly patterned with 25%, 50% and 75% duty cycles. The differential deformation before and after patterning was measured with the S-H metrology tool. The relative change of residual integrated stresses in oxide is presented as a normalized mean stress and plotted vs. duty cycle in Fig.7.

The points represent the measured data (five samples for each duty cycle) and the red line is a linear fit. As expected, the measured residual stress varies in proportion to the duty cycle. Lower duty cycle means less oxide is removed which leads to a higher residual stress. The 0.24% standard deviation of the data from the fit demonstrates excellent process control. This is expected due the high quality of thermal oxide and the high precision of the photo process.

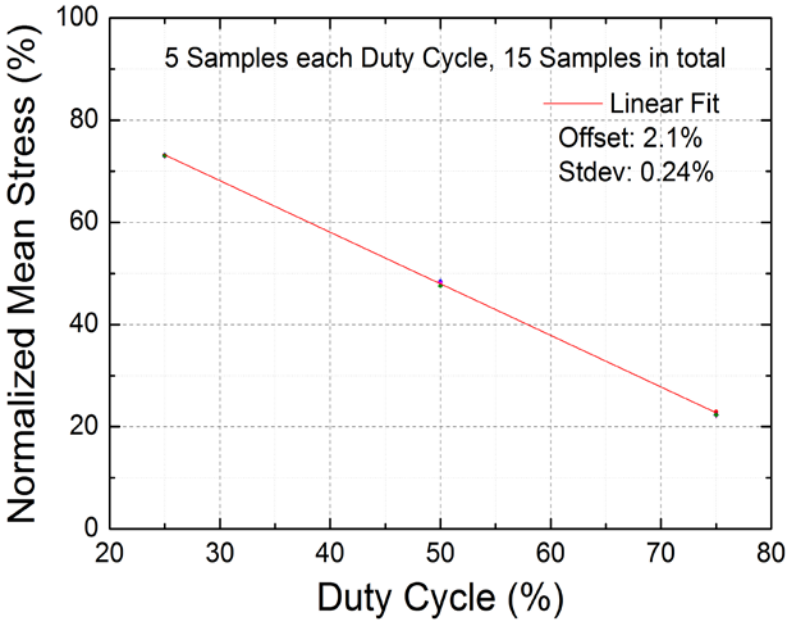

Figure 7. Calibration results of measured normalized mean stress versus duty cycle.

The 2.1% offset in the linear fit suggests a systematic error in our process. After inspection, we noticed that the plastic film photomasks had larger hexagon clear-out areas than designed. (Masks were patterned by an outside vendor.) A somewhat random area oversize of ~2.5% on average is seen which results in over etching of wafers. In order to solve this problem, we requested four masks printed by the vendor with a range of line-width bias (2.0-3.5% smaller) for each stress compensation trial on coated substrates. Before the exposure step, a microscope is used to select the mask closest to the design so the systematic error can be reduced and the other masks are discarded.

4. COMPENSATING COATING STRESS ON FLAT SILICON WAFERS

We applied the correction process to three 100 mm-diameter, 525 μm-thick silicon wafers to demonstrate compensation of coating stress and thereby recover the initial surface shape. Since an iridium target was not available for these initial experiments, the wafers were coated with 30 nm of sputtered chromium as substitute. The chrome was deposited in an RF magnetron using argon gas, with RF bias of ~-70 V at 10 W, which produces films with a compressive stress comparable to preferred iridium mirror coatings. The coated wafers were annealed in a tube furnace at 200 ℃ for 2 hours to stabilize the coating and eliminate stress relaxation. (We found that stress in sputtered chrome coatings that are not annealed tend to drift with time[10].) Measured surface distortions caused by the annealed coating and the corrected surfaces after compensation are shown in Fig. 8.

The surface maps in the left column of Fig. 8 show the distortion due to the metal coating, while those in the right column compare the final corrected mirror shape with the initial shape. Due to the compressive stresses, the coating distortions are convex. Note the scale change between the left and right columns. The calculated RMS heights and slope errors are presented in Table 1.

The results in Table 1 show that thermal oxide patterning significantly reduces coating-induced distortion on flat wafers. The RMS heights were improved by a factor of 100 and slope errors by a factor of 80. The wafer distortion after compensation, in terms of the slope error, is only about 0.4 arc-second, which is comparable to the measurement noise of our S-H metrology tool.

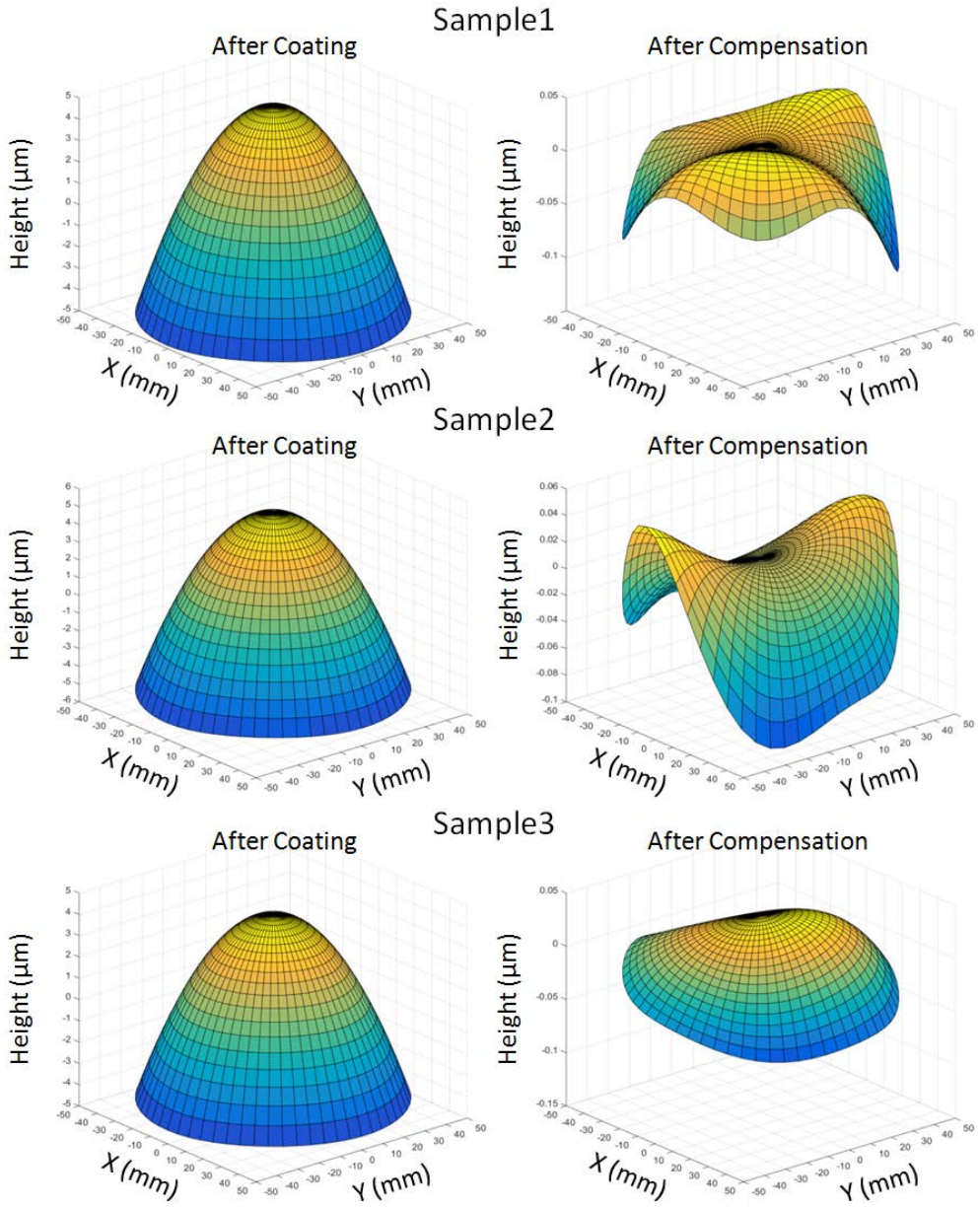

Figure 8.(Left column) Measured differential distortion maps comparing mirror surface before metal coating (Step. 2 in Fig. 1) and after metal annealing (Step 4 in Fig. 1). These maps show the distortion due to the annealed metal coating. (Right column) Measured differential distortion maps comparing mirror surface before oxidation (Step 0 in Fig. 1) and after compensation (Step. 5 in Fig. 1). Note the scale of the vertical axis in the right column is 100 times smaller than that in the left.

Table 1: RMS height and slope errors calculated from data in Fig. 9

	RMS Height (µm)		**RMS Slope Error (arc-second)**	
	Before Comp.	After Comp.	Before Comp.	After Comp.
Sample1	2.8	0.023	36.0	0.40
Sample2	2.9	0.028	36.9	0.44
Sample3	2.5	0.023	31.8	0.40

5. COMPENSATING COATING STRESS ON WOLTER MIRRORS

The thermal oxide patterning method was also applied on two samples of curved Wolter silicon mirrors[17] which were produced and coated with 30 nm of iridium by the Goddard group. The dimensions of the mirrors are 100 mm by ~80 mm by 0.75 mm, the mirror radius is 158 mm and the azimuthal span is 30 degrees. The coatings were also annealed at 200 °C for two hours to stabilize the stress. The surface shapes in each step were measured by an interferometer with a cylindrical null by the Goddard group. The measured surface profiles are shown in Fig. 9.

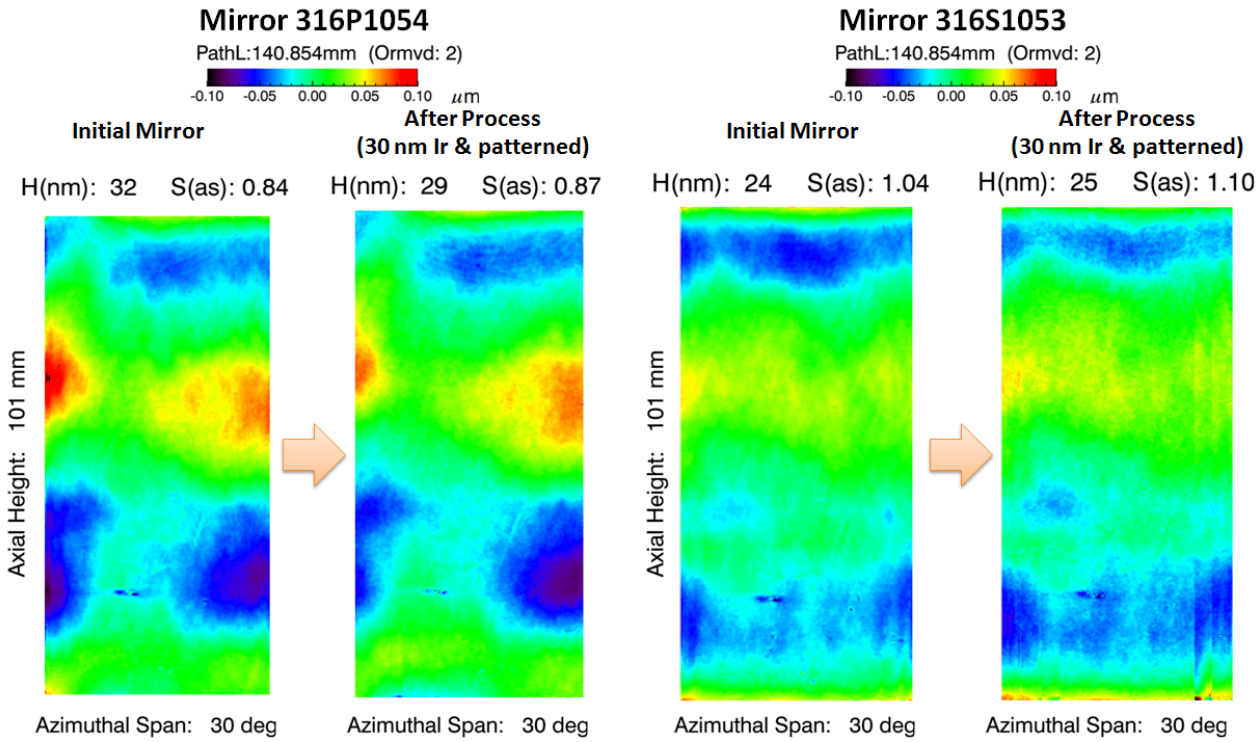

Figure 9. Measured surfaces of two Wolter mirrors corrected for metal coating distortion. H(nm) indicates the RMS height in nanometers and S(as) indicates the RMS slope error in arc-seconds. (Left two panels) Before/after results for Mirror 316P1054. (Right two panels) Before/after results for Mirror 316S1053.

The measured surface profiles are constructed by the best fit of Chebyshev polynomials (exclude 2nd order) on each column of raw data (axial direction) extracted from the interferometer in Goddard group. The surface maps marked "Initial Mirror" show the raw mirror surface just after polishing and before coating (Step 0 in Fig. 1), while the "After Process" maps show the same mirror surface after coating and oxide stress compensation. For both mirrors, the surface degradation in RMS slope error after the processes is less than 0.06 arc-second RMS axial slope, demonstrating a repeatable, high precision process.

6. CONCLUSIONS AND FUTURE WORK

A thermal oxide patterning method has been developed to compensate metal-induced distortion of silicon wafers and X-ray mirrors. The method is based on a stable thermal oxide layer and a simple photo lithography process on the back side of the substrate which is inexpensive and suitable for mass production. Stress calibration tests demonstrated that the method can control the local mean stress in oxide to a precision of <0.3%. Three flat silicon wafers coated with 30 nm of chromium with ~70 N/m compressive integrated stress were corrected, achieving a factor of 80 slope error improvement. In addition, two high-precision silicon Wolter mirrors were coated with 30 nm of compressive iridium and then

compensated by this process, returning the mirrors to their original figure to within 0.06 arc-second RMS axial slope. Thermal oxide patterning is a promising process for correcting mirror coating distortion for Lynx. In the future, the method will be further developed using thinner mirrors with higher surface quality.

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