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Thermal oxide patterning method for compensating coating stress in silicon substrates

YOUWEI YAO,[1,*] BRANDON D. CHALIFOUX,[1,2] RALF K. HEILMANN,[1] AND MARK L. SCHATTENBURG[1]

[1]*Space Nanotechnology Laboratory, Kavli Institute for Astrophysics and Space Research, Massachusetts Institute of Technology, Cambridge, MA 02139, USA*
[2]*Department of Mechanical Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139, USA*
**Yao.xray@gmail.com*

Abstract: We introduce a novel method for correcting distortion in thin silicon substrates caused by coating stress. Thin substrates, such as lightweight mirrors for x-ray or optical imaging, and semiconductor wafers or flat panel substrates, are easily distorted by stress in thin film coatings. We report a new method for correcting stress-induced distortion in flat silicon substrates which utilizes a micro-patterned silicon oxide layer on the back side of the substrate. Due to the excellent lithographic precision of the patterning process, we demonstrate stress compensation control to a precision of ~0.2%. The proposed process is simple and inexpensive due to the relatively large pattern features on the photomask. The correction process has been tested on flat silicon wafers that were distorted by 30 nm-thick compressively-stressed coatings of chromium, achieving RMS surface height and slope error reductions of a factor of 68 and 50, respectively.

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1. Introduction

The NASA Lynx x-ray telescope mission concept is currently under study for consideration by the 2020 Decadal Review [1]. The mission's ambitious goals include an angular resolution comparable to the NASA Chandra X-ray Observatory (0.5 arc-second) but with some 30x more collecting area and a much wider field of view [2]. To meet these goals, Lynx requires light-weight mirrors that are a factor of 40 thinner than Chandra's. Over the last decade many mirror concepts have been proposed [3]. The very successful NuSTAR mission has demonstrated that very thin mirrors can be successfully flown [4]. Lynx, however, will require similarly thin mirrors, but with resolution improved by a factor of over100.

A group at the NASA Goddard Space Flight Center (GSFC) has developed a process for producing thin silicon mirrors with high angular resolution (~1") using a relatively simple, low cost process [5]. These mirrors have come close to meeting requirements for Lynx, and rapid progress continues to be made. Unfortunately, preferred x-ray reflective coatings for mirrors, such as iridium, typically exhibit high compressive stress on the order of 1-3 GPa, which can distort the precisely-figured initial shape of the 0.5 mm-thick mirrors by many times the tolerance limit. In this paper we demonstrate an effective method for correcting coating stress distortion with very high precision.

The effective area of mirrors in the soft x-ray band (0.1-10 keV) relies on the performance of reflective coatings. Mirror coatings utilizing high-density elements enable increased critical angle of reflection and higher reflectivity for x-rays, thereby improving the telescope's throughput [6]. Sputter coating processes of materials onto substrates generally yield high quality films (e.g., dense, smooth, and fine grain) when the process is optimized for high compressive stress [7]. Many groups have attempted to produce high quality, low stress iridium films with limited success. A group at GSFC tried to relax the coating stress after

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deposition by annealing at 350 °C, but they found that the residual RMS slope error of coated wafers after annealing could not be improved to better than 1-2 arc-seconds [8], which is not compatible with Lynx requirements. They also attempted to balance the compressive stress in the iridium film by depositing chromium film under tensile stress beneath the iridium, or by using atomic layer deposition to coat iridium films on both sides of the mirror, but stress non-uniformity resulted in a poor balance and a 1-2 μm mirror sag error which is far beyond the Lynx requirement [9]. Another group, at the NASA Marshall Space Flight Center (MSFC), monitored stress in situ during deposition onto 50 mm-diameter flat silicon wafers, and was able to reduce the stress in 15 nm-thick iridium films to ~3 MPa (~0.05 N/m of integrated stress, i.e., the stress in the film integrated over its thickness, which is equivalent to the mean film stress multiplied by the film thickness) [10], which may meet Lynx requirements [11]. However, stress uniformity, stability and coating reflectivity are critical issues for this method and have not yet been sufficiently demonstrated. In addition, in situ coating stress measurement on Wolter-type mirrors requires improvements of their measurement system which have not yet been reported. Other groups are working on stress compensation ideas such as PZT active correction [12], ion-implantation [13] and stressed coatings on the backside of the mirrors [14,15], but a general and robust method has not been demonstrated.

A general method for correcting substrate distortion caused by high compressive film stress could potentially enable a new generation of high-performance x-ray mirrors which benefit from both excellent reflectivity enabled by high coating quality, and excellent figure provided by accurate stress compensation. In order to address distortion of silicon mirrors induced by coating stress, we have developed a new process which utilizes standard semiconductor processes. Based on the fact that thermal oxide grown on silicon substrates generates repeatable ~-300 MPa (compressive) stress [16,17], which is extremely stable, we developed a process to produce thermal oxide patterns on the backside of mirrors to compensate for coating stress.

2. Process

In this paper, we demonstrate a process for stress compensation of 100 mm diameter, 525 μm thick flat silicon wafers distorted by 30 nm thick chromium coatings. For future work we will apply this process to thin x-ray mirrors, which are curved (Wolter geometry). We selected chromium for this work as a substitute for iridium simply because it is inexpensive and readily available in our lab.

The process flow is shown in Fig. 1. Silicon wafers (Step 0) are thermally oxidized in O_2 for three hours at ~1140 °C to grow 250 nm oxide on both sides (Step 1). This results in an integrated stress of around −75 N/m (compressive), which is slightly larger than the chrome coating's expected integrated stress to be compensated. The oxide thickness can easily be adjusted to modify the integrated stress for different coatings. After oxidation, in Step 2 the wafer's front side is measured to provide an initial surface profile map, M_1. (See Section 2.1.1 for details of our surface metrology tool.) We have found that the surface profile map measured before and after oxidation hardly changes due to the excellent oxide uniformity.

After oxidation, in Step 3 the wafer's back side is spin-coated with Dow SPR-700 photoresist (PR) and baked. The wafer is then dipped into 1:7 buffered oxide etch (BOE) to remove the front side oxide film. Then the PR is removed by Piranha. Since the oxide film's compressive stress vanishes when dissolved in the chemical, the wafer bows until it reaches equilibrium. In Step 4 the wafer's front side is again measured to provide a second surface profile map, M_2. The difference between the surface maps obtained in Steps 2 and 4, given by $M_{\text{oxide}} = M_2 - M_1$, is then used to derive an integrated stress map of the back side oxide layer. See Section 2.1.2 for details of our methodology to determine film stress from surface topology maps.

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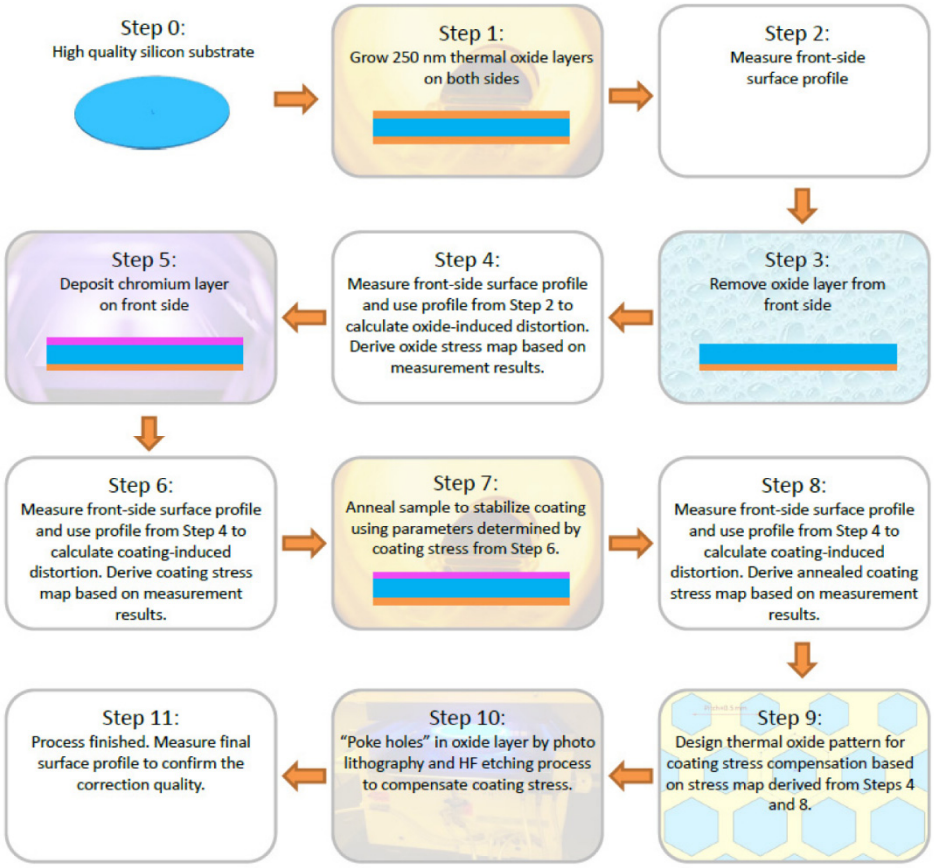

Fig. 1. Process for stress compensation by thermal oxide patterning. Boxes with white backgrounds indicate metrology steps.

Next, the wafer is cleaned in piranha solution and placed into a magnetron sputtering system to deposit 30 nm of chromium on the front side (Step 5). During deposition, the working gas (argon) pressure is stabilized at 3 mTorr [18], and a negative RF (Radio Frequency) bias voltage with constant power (10 W) [14] is applied to generate around −70 N/m compressive stress, which is similar to that of iridium coatings for telescope mirrors [8,9]. In Step 6, the wafer's front side is again measured to provide a third surface profile map, M_3. This is used to determine the integrated stress map of the coating from $M_{\text{coating}} = M_3 - M_2$.

After Step 6, since the integrated stresses on both sides are similar, the wafer distortion should be somewhat alleviated. In Step 7 a thermal annealing cycle is performed, which is described in more detail in Section 2.2. The annealing conditions are carefully selected to ensure that (1) the coating stress is stable, (2) its integrated stress is lower than the oxide, and (3) its surface quality is not degraded [9]. In Step 8 the wafer's surface profile is again measured to provide a fourth surface profile map, M_4. This is used to determine the integrated stress map of the coating after annealing from $M_{\text{annealed}} = M_4 - M_2$. Please see section 2.2 for details of our coating stress stabilization methodology. For a mature and repeatable coating process (as would be needed for Lynx) M_3 could be omitted.

In Step 9, a high precision lithographic pattern is designed that will be subsequently transferred into the oxide layer by chemical etching. We have chosen a repeating hexagonal pattern shown in Fig. 2, although other patterns could be used. The pattern is chosen so that the entire substrate is covered by a repeating hexagonal unit cell with a constant pitch of 0.5

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mm, but where the ratio of etched area to oxide-covered area varies within each cell. Since the voided area varies in size while the period is fixed, the modulation of the pattern is similar to that of pulse width modulation (PWM) in electronics. We define the ratio between the area of an etched hexagon, and that of a unit cell, as the duty cycle. Please see Section 2.3 for details of our pattern design methodology. Maps M_1, M_2, and M_4 are used to design a duty cycle map which is used to generate a masking pattern, as depicted in Fig. 2, where yellow areas (where oxide remains) are represented on the photomask by an ink layer, which blocks UV light, while blue areas (where oxide is to be removed) are represented on the mask by open areas.

The hexagon pitch is fixed at 0.5 mm for two reasons. First, sub-mm features are smaller than the wafer thickness which helps prevent print-through distortion. Second, sub-mm scale structures are less difficult to fabricate than, for example, micron scale features. The sizes of etched hexagons are adjusted within a unit cell, which is the maximum boundary shown by the gray dashed lines in Fig. 2. By adjusting the duty cycle locally, the mean stress within a unit cell can be precisely controlled. In this manner, the equivalent stress on the back side of the wafer can be locally tuned to match the local integrated stress of the coating, allowing accurate compensation for spatially varying film stress or thickness and enabling the surface profile of the coated wafer to recover the initial shape. A similar method has been used to generate non-uniform integrated stress using ion implantation [19].

In Step 10, the wafer back side is again spin coated with PR, brought into intimate contact with the photomask, and exposed with UV light. (See Section 2.4 for details of the photolithography process.) The latent image in the PR is then etched in developer solution, the wafer is rinsed and dried, and then etched in BOE, thereby "poking holes" in the oxide layer. The lithographic release of stress then compensates the distortion caused by the coating stress. In Step 11 the surface is again measured to confirm successful correction, generating map M_5. An error map of the process, which represents the failure of the patterned oxide to perfectly correct for coating distortion, can be obtained from $M_{\text{error}} = M_5 - M_1$.

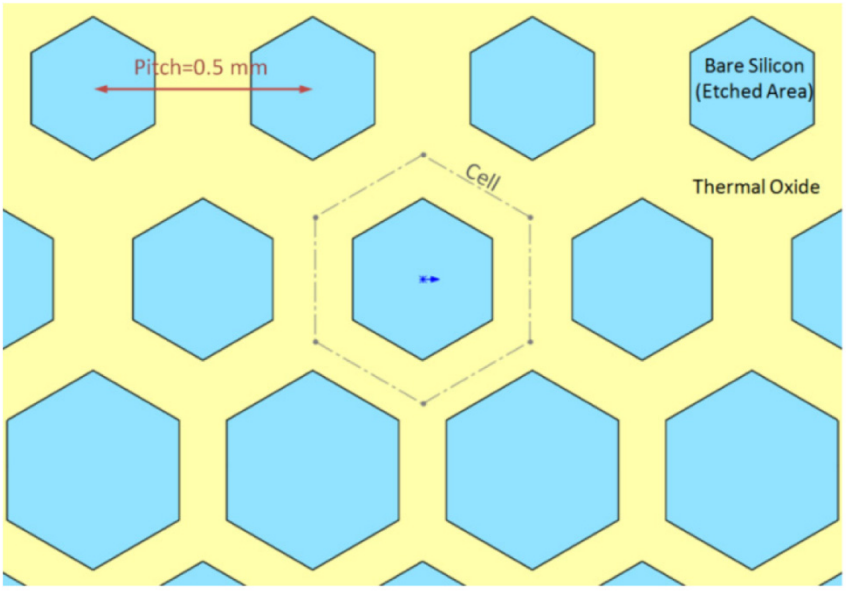

Fig. 2. Sketch of thermal oxide pattern. A hexagonal unit cell (grey dashed lines) with 0.5 mm face-to-face width is used. In this illustration the pattern duty cycle increases from top to bottom, representing a stress (or thickness) gradient. Yellow regions indicate intact 250 nm-thick oxide coating, while the blue hexagonal regions indicate open areas where oxide has been removed (bare silicon surface).

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2.1 Metrology

2.1.1 Shape metrology

The lithographic pattern is designed based on calculated stress distributions in the coating and oxide layers, which are derived from wafer surface metrology. Therefore, the metrology system is crucially important. We use a Shack-Hartmann (S-H) metrology tool in our lab to measure wafer surface topology [20]. The tool is covered with a plastic enclosure to reduce measurement error caused by turbulence. The sample holder has been designed to minimize distortion induced by gravity and clamping [21]. Zernike polynomials are fit to the measured surface slopes, and the relative displacement of the wafer surface between multiple process steps can be reconstructed. Measurement noise is typically ~1-10 nm RMS in each Zernike term, and ~20 nm RMS in total, corresponding to a ~0.35 arc-second slope error on a 100 mm-diameter wafer [13]. Please see Table 3 for more details of the noise floor.

Figure 3 shows an example of measured surface displacement between Steps 1 and 2 shown in Fig. 1, which demonstrates the distortion induced by the compressive thermal oxide layer on the back side of the wafer.

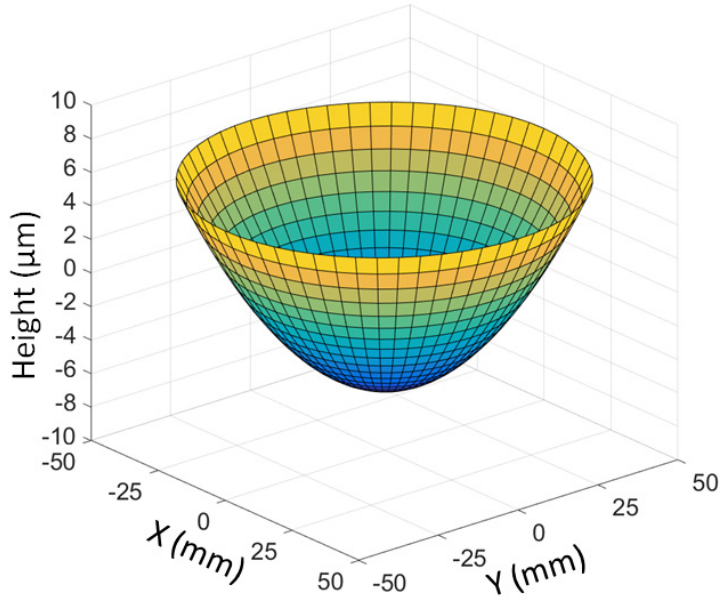

Fig. 3. Measured surface distortion induced by a thermal oxide layer on the backside of the wafer, which is represented by the Zernike polynomial coefficients provided in Table 1.

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Table 1. Calculated Zernike coefficients and corresponding terms (Noll ordering)

Coefficient (μm)	Zernike term
3.525×10^{0}	a_4 (spherical: Z_2^0)
3.171×10^{-4}	a_5 (astigmatism: Z_2^{-2})
9.460×10^{-4}	a_6 (astigmatism: Z_2^2)
1.068×10^{-2}	a_7 (coma: Z_3^{-1})
1.017×10^{-2}	a_8 (coma: Z_3^1)
-9.31×10^{-3}	a_9 (trefoil: Z_3^{-3})
4.535×10^{-3}	a_{10} (trefoil: Z_3^3)
7.165×10^{-3}	a_{11} (2nd spherical: Z_4^0)
-6.193×10^{-6}	a_{12} (2nd astigmatism: Z_4^{-2})
1.023×10^{-3}	a_{13} (2nd astigmatism: Z_4^2)
2.769×10^{-3}	a_{14} (quadrafoil: Z_4^{-4})
8.141×10^{-4}	a_{15} (quadrafoil: Z_4^4)

In Table 1 the coefficients a_0, a_1 and a_2 represent piston, tip and tilt, which do not affect the surface and have been omitted. Note the coefficient of the a_4 spherical term is much larger than the others implying the stress in the thermal oxide is very uniform.

2.1.2 Stress calculation

Based on the Zernike coefficients of the measured deformation, the stress distribution of the coating and thermal oxide can be derived, which has been demonstrated previously [19,22]. The stress distribution is considered as a linear combination of stress functions which are also represented by normalized Zernike polynomials. We build a finite element (FE) model using commercial software (ADINA) to calculate the wafer surface deformation induced by these stress functions, fit the calculated deformations with Zernike polynomials, and record the fitted coefficients in an array library. The correlation between the measured Zernike coefficients, the stress function coefficients and the array library is determined by the following equation

$$\begin{bmatrix} C_{11} & \cdots & C_{1K} \\ \vdots & \ddots & \vdots \\ C_{N1} & \cdots & C_{NK} \end{bmatrix} \begin{bmatrix} b_1 \\ \vdots \\ b_K \end{bmatrix} = \begin{bmatrix} a_1 \\ \vdots \\ a_N \end{bmatrix} \tag{1}$$

Where a_i are the measured Zernike coefficients of deformation. Array C is the library in which each element stores a Zernike coefficient derived from an FE model. The model is based on a 100 mm diameter and 525 μm thick silicon wafer with a 1 μm oxide coating on the back side (the oxide thickness can be set arbitrarily since the calculated integrated stress of oxide for a measured distortion is independent of the oxide layer thickness). In this model, 15 terms of Zernike coating stress functions were applied. The 15 calculated deformations are fitted by Zernike polynomials, and the coefficients of each deformation are stored in each column of array C. Therefore, in Eq. (1), K = 15 is the total number of Zernike stress functions tested by the FE model, and b_i are the coefficients of Zernike stress functions to be solved using the pseudo inverse method in MATLAB. Figure 4 shows the reconstructed stress distribution in thermal oxide based on the measurement shown in Fig. 3.

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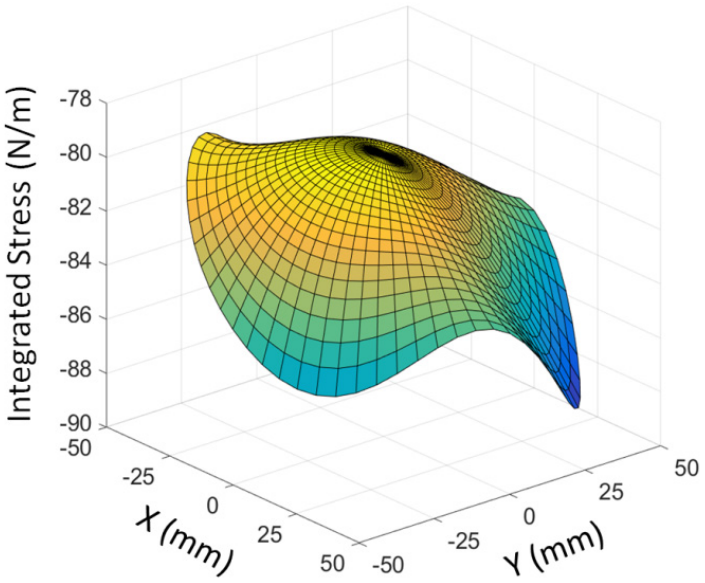

Fig. 4. Calculated stress distribution in a thermal oxide layer. The mean integrated stress is −82 N/m (compressive) with a standard deviation of 1.96 N/m, indicating good uniformity.

2.2 Coating stress stabilization

Wafers were coated with 30 nm of chromium using a magnetron sputtering system. During deposition, a negative RF bias voltage with 10 W power is applied to the wafer to impart approximately −70 N/m (compressive) stress to emulate typical iridium coatings for telescope mirrors. We observed that coating stress measured right after deposition was not stable. Over a period of weeks, the coating stress showed significant relaxation, which could cause large stress compensation errors. To address this problem, we developed a thermal annealing process applied after deposition to accelerate the relaxation and stabilize the stress.

For our process, annealing temperatures of at least 200 °C are preferred so as to be at least 50 °C higher than the photo-lithography bake step. Temperatures are also preferred to be under 300 °C to prevent surface degradation [9]. All annealing trials were conducted at 200 °C or 300 °C for two hours in N_2. In order to demonstrate effective annealing, we coated 10 silicon wafers with chromium under identical sputtering conditions, and then tracked their mean stresses for several weeks. Samples 6-10 were annealed at 200 °C and monitored twice (right after annealing and 20 days later), while Samples 1-5 were not annealed, and were monitored every two days. Results are shown in Fig. 5. The stresses shown in the plot were either normalized to the stress measured right after deposition (Samples 1-5), or to the stress measured right after annealing (Samples 6-10). The stresses are all calculated from the spherical term a_4 derived from the S-H surface height map. For wafers that were not annealed, stresses relaxed by about 5% over two weeks after deposition. On the other hand, the annealed coatings were much more stable. In this case the scatter of the mean stress data is only ~0.5% (8 nm RMS height change in spherical term a_4), which is comparable to our measurement noise.

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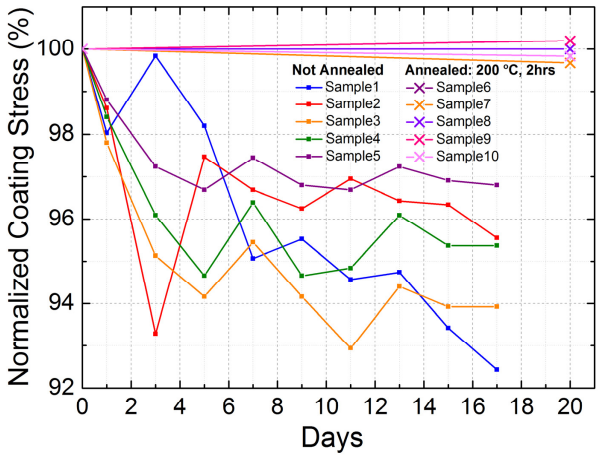

Fig. 5. Measured stress relaxation in a 30 nm-thick chromium coating with and without annealing (2 hours at 200 °C in N_2). Non-annealed coatings experience several percent relaxation per week. Annealed samples display constant stress (within measurement noise). Each data point represents one measurement on a wafer.

As noted previously, the thermal oxide patterning method compensates coating stress by means of compressive stress in the thermal oxide. During the coating process we noticed that the compressive stress in the chrome layer produced by a fixed bias voltage varied over 20% for different samples. If the coating stress is higher than the oxide stress, then the capacity of the compensation will be limited. In this case, during annealing the temperature is increased to reduce the coating stress to within the capture range of the lithographic process, which is approximately 50% of the oxide stress. In order to identify the capability to reduce the stress, we coated seven silicon wafers, annealed five of them at 200 °C and the remainder at 300 °C. The samples were annealed for multiple cycles, and stresses were monitored after each cycle, with results shown in Fig. 6.

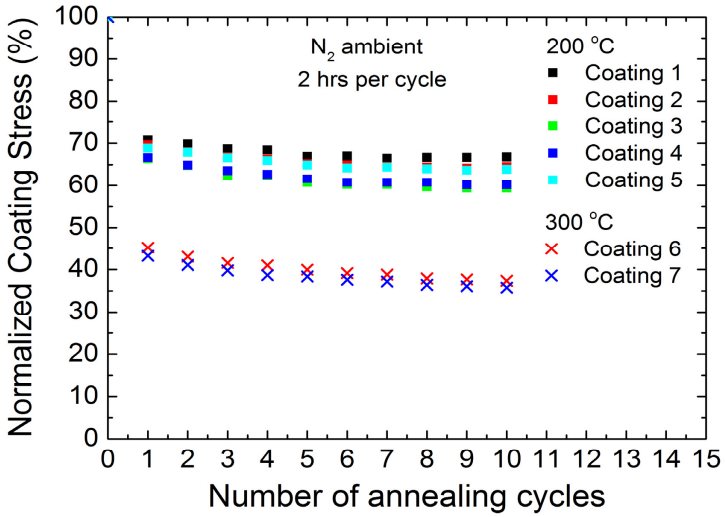

Fig. 6. Measured stress relaxation in 30 nm-thick chrome coatings vs. number of two-hour thermal cycles for temperatures of 200 °C and 300 °C.

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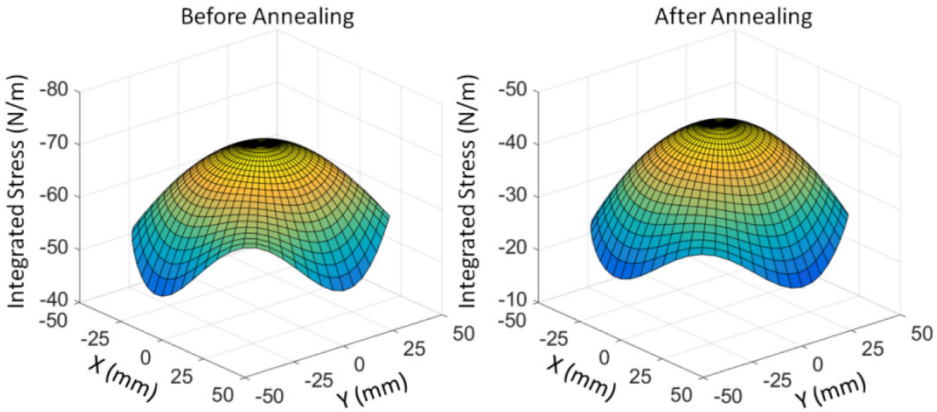

Fig. 7. Coating stress of a 30 nm chromium layer on a wafer front side measured before (left) and after (right) annealing at 200 °C.

For these temperatures most of the stress relaxations occur in the first thermal cycle indicating a two-hour annealing time is appropriate. Reduction of coating stress was ~30% and ~55% for 200 °C and 300 °C cycles, respectively. These results help to determine the optimal annealing temperature based on the measured mean stress in the coating and thermal oxide. Figure 7 shows an example of integrated coating stress measured before and after annealing, where coating stress was reduced by ~35% to a mean stress of −35.08 N/m, which is about half of the oxide stress. Comparing this data to Fig. 4, we note that the integrated coating stress is not as uniform as in the oxide, showing coating stress relaxation at the rim that is higher (in percentage) than that at the center, which implies the thermal oxide pattern for stress compensation should have a higher duty cycle at the rim. In order to correct the wafer distorted by this coating stress, an oxide pattern has been designed, as described in the next section.

2.3 Pattern design

In the oxide pattern, the size of each hexagon hole is determined by a duty cycle map. The pattern's local duty cycle is proportional to the area of oxide to be removed, which can be calculated from the measured stress maps of the thermal oxide and the annealed coating using the following equation:

$$Duty\ Cycle(x,y) = \frac{S_{oxide}(x,y) - S_{annealed}(x,y)}{S_{oxide}(x,y)} \tag{2}$$

Where $S_{oxide}(x,y)$ is the integrated stress map derived from $M_{oxide} = M_2 - M_1$, and $S_{annealed}(x,y)$ is the map derived from $M_{annealed} = M_4 - M_2$. For example, Fig. 8 shows a calculated duty cycle map based on the oxide and annealed coating stresses shown in Figs. 4 and 7, respectively.

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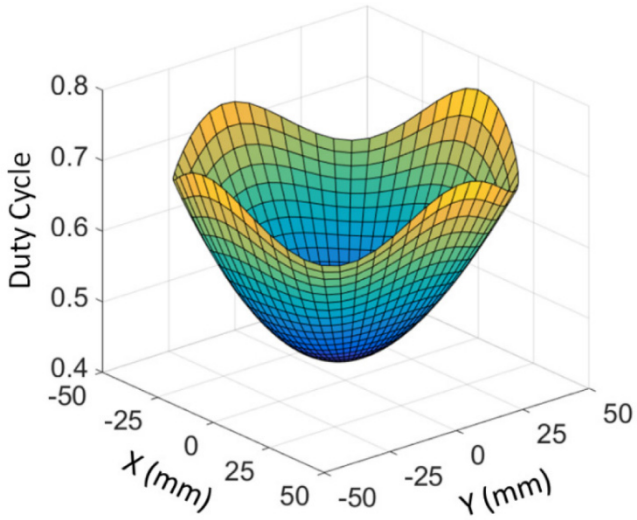

Fig. 8. Example of a duty cycle map calculated from maps shown in Figs. 4 and 7.

We generate the hexagon pattern as an AutoCAD DXF file. A photomask vendor can then produce a thin plastic photomask (see Fig. 9), which is subsequently printed as described in Section 2.4. A plastic photomask substrate was chosen due to low cost and ease of conformal contact with substrates.

2.4 Photo-lithography process

The hexagon pattern in thermal oxide is fabricated using the following steps. First, the wafer with oxide and annealed chrome layer is baked at 150 °C for 10 min to dehydrate the surface. Since this temperature is at least 50 °C lower than the annealing temperature, the coating stress does not change. Second, the backside of the wafer with thermal oxide layer is spin coated with Dow SPR-700 PR. The spin speed is set to 3000 RPM to yield a PR thickness of ~1 μm. Third, the wafer is baked at 110 °C for 3 minutes to harden the PR.

Fig. 9. Plastic film photomask with hexagon pattern. The inset (upper right corner) shows the hexagon pattern observed under a microscope.

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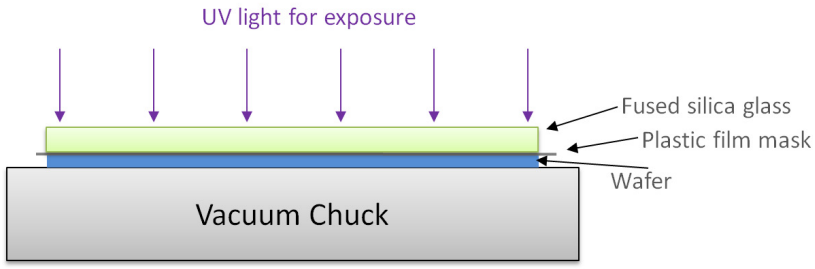

Fig. 10. Diagram of the exposure process in the photo printer.

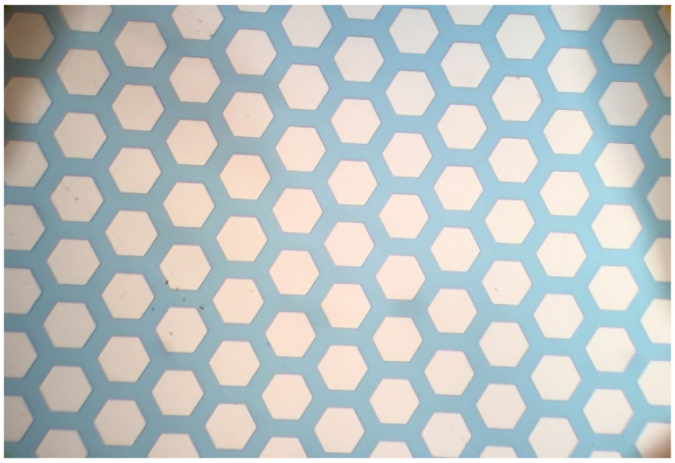

Fig. 11. Optical micrograph of fabricated thermal oxide pattern. The blue area is thermal oxide and white hexagons are exposed silicon. In this example, the oxide is blue in color since the thickness is ~150 nm for test purpose.

Fourth, the photomask is aligned with the wafer and hard contact printed into the PR with UV light (365 nm and 406 nm wavelength) as shown in Fig. 10. Since the hexagons on the mask are transparent, the PR within these areas is exposed and can subsequently be removed in a developer solution (Microposit MF CD-26). Therefore, a PR layer with hexagon voids is created on top of the thermal oxide. In a fifth step, the sample is dipped into buffered oxide etch (BOE) for 5 minutes so the oxide within the hexagons is thoroughly removed. In the last step, the sample is soaked in acetone, removing the PR and any organic contaminants from both sides of the wafer. After these steps, a thermal oxide pattern remains as shown in Fig. 11.

3. Calibration

The fabrication process has multiple steps which could introduce errors into the stress compensation. Before correcting chrome-coated wafers, calibration tests were performed to study the precision that can be achieved and to improve the process to minimize systematic errors. In this test, 15 wafers with single-side oxide coatings were divided into three groups of five and each group patterned directly with duty cycles of 25%, 50% and 75%. In each group a mask with constant duty cycle pattern across the surface was used to generate uniform stress. The mean residual integrated stress on each wafer was measured and normalized by the integrated stress measured before etching. The results are plotted vs. duty cycle and shown in Fig. 12.

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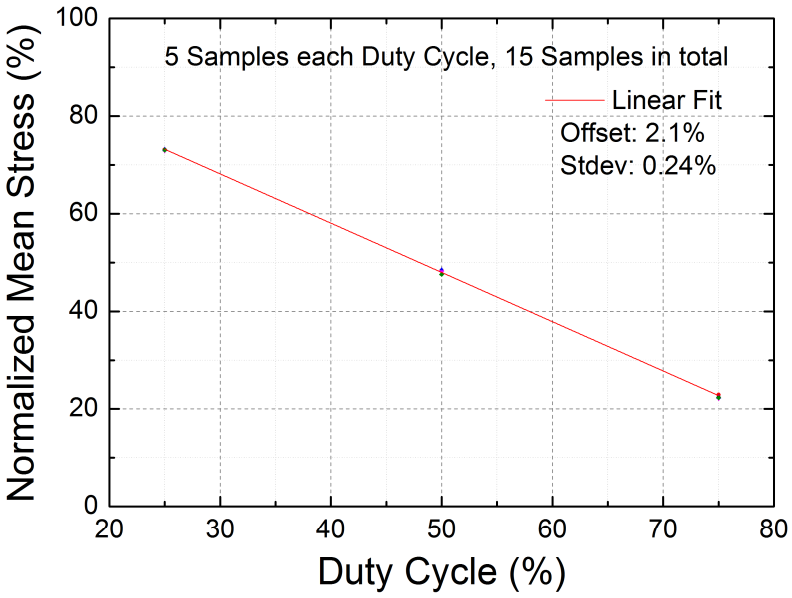

Fig. 12. Calibration test: measured mean integrated stress vs. designed duty cycle.

As expected, the mean integrated stress of the fabricated oxide pattern varies linearly with the designed duty cycle. The standard deviation derived from a linear fit indicates that the mean stress is controlled to within a very high precision of ± 0.24%. In addition, the fit resulted in an offset of 2.1%, which suggests there is a systematic over-etching in the process. After microscopic inspection, we found that the patterns on the plastic photomask had hexagons that were on average 2.5% larger than the designed hexagons, which resulted in over-etching of all 15 wafers. We also found that the pattern error varies from mask to mask, which may be worse for printed plastic photomasks than for chrome-on-glass photomasks. For stress compensation of chrome-coated wafers, we procured four masks with patterns undersized by 2% to 3.5% and selected the mask with the least over-size error.

4. Results

The process was then applied on three wafers to compensate for coating stress and recover the initial surface shape. Figure 13 shows the measured deformation (differences relative to the initial shape) of samples distorted by the coating (left) and after correction (right). The calculated RMS height and slope errors are shown in Table 2.

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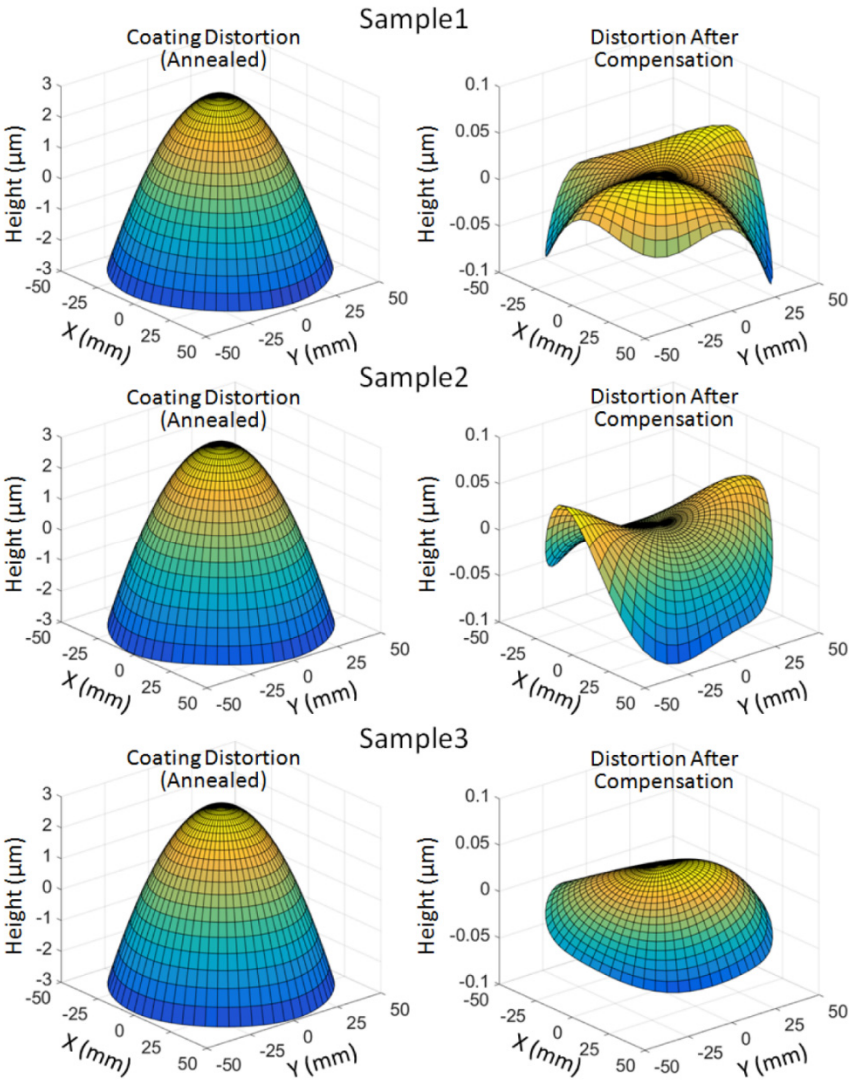

Fig. 13. Measured surface distortion after coating (left) and after stress compensation (right). Note 30x smaller vertical scale in the right side. For Sample1, the measured thermal oxide stress was shown in Fig. 4, the coating stress in Fig. 7 and the calculated duty cycle in Fig. 8.

Table 2. RMS height and slope errors of the wafer distortion measured before and after compensation, derived from data shown in Fig. 13

	RMS Height (µm)		RMS Slope Error (arc-second)	
	Before Comp.	After Comp.	Before Comp.	After Comp.
Sample1	1.63	0.023	20.9	0.40
Sample2	1.69	0.028	21.75	0.44
Sample3	1.67	0.023	21.45	0.40

The results in Table 2 show that wafer distortion induced by a coating can be significantly reduced by the thermal oxide compensation method. For the three samples the average improvement factor is 68 in terms of the RMS height and 52 in terms of surface slope. With an integrated coating stress of ~-40 N/m, which represents a typical iridium coating for x-ray telescopes after annealing, the slope error of wafer surface distortion after compensation is

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only ~0.4 arc-second which corresponds to 0.8 N/m residual stress after compensation. Since the Lynx mission requires a 0.5 arc-second mission level resolution, which has to be divided into terms for the primary and secondary mirrors and many other error terms, a 0.1 N/m residual stress for a 0.5 mm-thick single mirror may be necessary [11]. By looking into the Zernike coefficients of the three samples after compensation shown in Table 3, the residual distortions are dominated by the spherical and astigmatism terms which are possibly caused by systematic errors from the metrology and fabrication process. By replacing the S-H tool with an interferometer with 10x better precision and improving the fabrication process in the future, the requirement for Lynx might be achieved.

Table 3. Zernike coefficients of the residual distortion measured after compensation, derived from data shown in Fig. 13 (right)

Coefficient x 10^{-3} (μm)				Zernike term
Sample1	**Sample2**	**Sample3**	**Noise**	
−12.28	−12.56	−21.32	9.26	a_4 (spherical: Z_2^0)
−15.06	8.90	7.45	7.90	a_5 (astigmatism: Z_2^{-2})
−3.30	−21.33	−2.29	10.71	a_6 (astigmatism: Z_2^2)
0.36	−1.47	−0.99	1.89	a_7 (coma: Z_3^{-1})
−2.05	−3.39	−4.19	2.74	a_8 (coma: Z_3^1)
−4.40	2.36	−3.11	6.43	a_9 (trefoil: Z_3^{-3})
1.51	−1.66	−0.86	3.18	a_{10} (trefoil: Z_3^3)
−4.54	−4.18	−0.56	1.78	a_{11} (2nd spherical: Z_4^0)
0.32	1.18	0.12	1.78	a_{12} (2^{nd} astigmatism: Z_4^{-2})
2.94	0.83	−1.7	2.10	a_{13} (2^{nd} astigmatism: Z_4^2)
8.84	7.49	1.54	1.80	a_{14} (quadrafoil: Z_4^{-4})
3.29	−2.97	1.09	1.55	a_{15} (quadrafoil: Z_4^4)

5. Conclusion

We have developed a new thermal oxide patterning method for compensating thin substrates for coating stress distortion. We demonstrated this process by the recovery of the initial shape of silicon wafers distorted by thin metal coatings with integrated stresses typical of x-ray telescope mirrors. As part of this effort we developed a thermal annealing process to stabilize the stress of thin chromium coatings on silicon substrates. We also developed a calibration technique which allows for the measurement and correction of photomask errors. The calibration experiments demonstrated an integrated stress correction precision of approximately ± 0.2%. We demonstrated the complete process by compensating coating stresses on three wafers, confirming that the distortion induced by the coating stress can be reduced by a factor of 68 in RMS height, and 50 in RMS slope error. For these three wafers an average residual slope error after compensation of 0.4 arc-second was achieved, demonstrating the potential of this method for next generation x-ray telescopes.

For future work, we plan to extend the current process to thin silicon Wolter-type x-ray telescope mirrors which have parabolic shapes. Since the Zernike polynomials and our flat surface metrology tool are no longer applicable for curved mirrors, a new measurement system and pattern designed for Wolter mirrors are under development.

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References

1. J. A. Gaskin, A. Dominguez, K. Gelmis, J. Mulqueen, D. Swartz, K. McCarley, F. Özel, A. Vikhlinin, D. Schwartz, H. Tananbaum, G. Blackwood, J. Arenberg, W. Purcell, and L. Allen, "The Lynx x-ray observatory: concept study overview and status," Proc. SPIE **10699**, 106990N (2018).
2. M. C. Weisskopf, S. L. O'Dell, and L. P. Van Speybroeck, "Advanced x-ray astrophysics facility (AXAF)," Proc. SPIE **2805**, 2–7 (1996).
3. S. L. O'Dell, R. Allured, A. O. Ames, M. P. Biskach, D. M. Broadway, R. J. Bruni, D. N. Burrows, J. Cao, B. D. Chalifoux, K. Chan, Y. Chung, V. Cotroneo, R. F. Elsner, J. A. Gaskin, M. V. Gubarev, R. K. Heilmann, E. Hertz, T. N. Jackson, K. Kilaru, J. J. Kolodziejczak, R. S. McClelland, B. D. Ramsey, P. B. Reid, R. E. Riveros, J. M. Roche, S. E. Romaine, T. T. Saha, M. L. Schattenburg, D. A. Schwartz, E. D. Schwartz, P. M. Solly, S. Trolier-McKinstry, M. P. Ulmer, A. Vikhlinin, M. L. Wallace, X. Wang, D. L. Windt, Y. Yao, S. Ye, W. W. Zhang, and H. Zuo, "Toward large-area sub-arcsecond x-ray telescopes II," Proc. SPIE **9965**, 996507 (2016).
4. W. W. Zhang, "Manufacture of mirror glass substrates for the NuSTAR mission," Proc. SPIE **7437**, 74370N (2009).
5. W. W. Zhang, K. D. Allgood, M. P. Biskach, K. Chan, M. Hlinka, J. D. Kearney, J. R. Mazzarella, R. S. McClelland, A. Numata, R. E. Riveros, T. T. Saha, and P. M. Solly, "Astronomical x-ray optics using mono-crystalline silicon: high resolution, light weight, and low cost," Proc. SPIE **10699**, 10699 (2018).
6. E. Spiller, *Soft x-ray optics* (SPIE, 1994), Chap. 7.
7. H. Windischmann, "Intrinsic stress in sputter-deposited thin films," Crit. Rvs. in Solid State & Mater. Sci. (Wroclaw) **17**(6), 547–596 (1992).
8. K. Chan, W. W. Zhang, D. Windt, M. Hong, T. Saha, R. McClelland, M. Sharpe, and V. H. Dwivedi, "Reflective coating for lightweight x-ray optics," Proc. SPIE **8443**, 84433S (2012).
9. K. Chan, M. Sharpe, W. W. Zhang, L. Kolos, M. Hong, R. McClelland, B. Hohl, T. Saha, and J. Mazzarella, "Coating thin mirror segments for lightweight x-ray optics," Proc. SPIE **8861**, 88610X (2013).
10. D. M. Broadway, J. Weimer, D. Gurgew, T. Lis, B. D. Ramsey, S. L. O'Dell, M. Gubarev, A. Ames, and R. Bruni, "Achieving zero stress in iridium, chromium and nickel thin films," Proc. SPIE **9510**, 95100E (2015).
11. B. D. Chalifoux, Y. Yao, R. K. Heilmann, and M. L. Schattenburg, "Simulation of film stress effects on angular resolution for the Lynx x-ray observatory concept," in preparation.
12. C. T. DeRoo, R. Allured, V. Cotroneo, E. N. Hertz, V. Marquez, P. B. Reid, E. D. Schwartz, A. A. Vikhlinin, S. Trolier-McKinstry, J. Walker, T. N. Jackson, T. Liu, and M. Tendulkar, "Deterministic figure correction of piezoelectrically adjustable slumped glass optics," J. Astron. Telesc. Instrum. Syst. **4**(1), 019004 (2018).
13. B. D. Chalifoux, Y. Yao, H. E. Zuo, R. K. Heilmann, and M. L. Schattenburg, "Compensating film stress in silicon substrates for Lynx x-ray telescope mission concept using ion implantation," Proc. SPIE **10699**, 1069959 (2018).
14. Y. Yao, X. Wang, J. Cao, and M. Ulmer, "Stress manipulated coating for fabricating lightweight X-ray telescope mirrors," Opt. Express **23**(22), 28605–28618 (2015).
15. H. Mori, T. Okajima, W. W. Zhang, K. Chan, R. Koenecke, J. R. Mazzarella, A. Numata, L. G. Olsen, R. E. Riveros, and M. Yukita, "Reflective coatings for the future x-ray mirror substrates," Proc. SPIE **10699**, 1069941 (2018).
16. E. Kobeda and E. A. Irene, "SiO_2 film stress distribution during thermal oxidation of Si," J. Vac. Sci. Technol. B **6**(2), 574–578 (1988).
17. Y. Nishi and R. Doering, *Handbook of Semiconductor Manufacturing Technology* (CRC, 2000), Chap. 7.
18. D. W. Hoffman and J. A. Thornton, "Internal stresses in sputtered chromium," Thin Solid Films **40**, 355–363 (1977).
19. B. D. Chalifoux, E. Sung, R. K. Heilmann, and M. L. Schattenburg, "High-precision figure correction of x-ray telescope optics using ion implantation," Proc. SPIE **8861**, 88610T (2013).
20. C. R. Forest, C. R. Canizares, D. R. Neal, M. McGuirk, and M. L. Schattenburg, "Metrology of thin transparent optics using shack-hartmann wavefront sensing," Opt. Eng. **43**(3), 742–753 (2004).
21. M. Akilian, C. R. Forest, A. H. Slocum, D. L. Trumper, and M. L. Schattenburg, "Thin optic constraint," Precis. Eng. **31**(2), 130–138 (2007).

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22. E. S. Claflin and N. Bareket, "Configuring an electrostatic membrane mirror by least-squares fitting with analytically derived influence functions," J. Opt. Soc. Am. A **3**(11), 1833–1839 (1986).

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